A Small Dual Mixer Time Difference (DMTD) Clock Measuring System

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Introduction

This paper describes a small and relatively simple Dual Mixer Time Difference (DMTD) clock measuring system (see Figure 1). A DMTD system is a well-established way to make high resolution phase measurements on precision frequency sources. This system is intended mainly for experimental purposes, but can be used to make low-noise measurements on up to three clocks versus a reference at the same nominal frequency in the range of 1-20 MHz. The system has a resolution of 20 femtoseconds for a 10 Hz beat frequency at an RF frequency of 10 MHz as shown in Figure 2. It has achieved a coherent noise floor below $1x10^{-13}$ at 1 second without phase averaging or cross-correlation, as shown in Figure 3, and well below that with cross-correlation. The design and implementation of the system hardware is described in detail. See Appendix I for a table of specifications for the Small DMTD Clock Measuring System.

Figure 1. The Small DMTD System

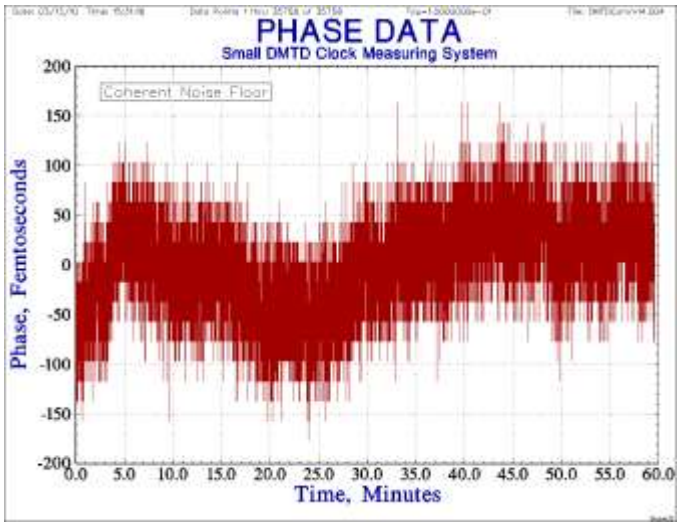


Figure 2. Small DMTD System Phase Data

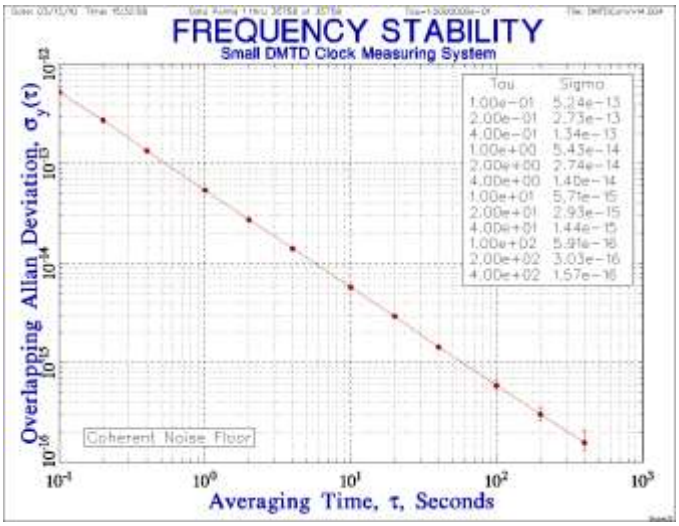


Figure 3. Small DMTD System Frequency Stability

DMTD System Description

The system has two mixer modules, each with dual mixers having RF and offset LO inputs whose low-passed outputs are amplified and processed by zero-crossing detectors to produce start and stop signals for two time interval counter modules. The offset LO signals are generated by a direct-digital synthesizer (DDS) module from a 10 MHz reference. The system also includes a pair of RF power splitters. This basic system, shown in the block diagram of Figure 4 and the photographs of Figure 5, can be configured in several ways to make coherent system noise tests, measurements on one or two pairs of clocks, and cross-correlation measurements on one pair of clocks. The system includes a Windows® PC program to capture data via a USB interface for subsequent analysis with Stable32.

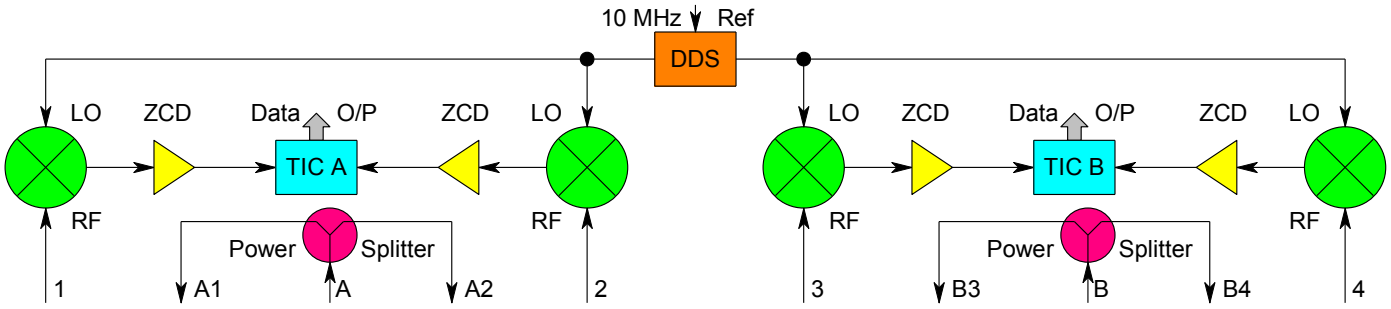


Figure 4. Block Diagram of Small DMTD Clock Measuring System

Table 1. Small DMTD Clock Measuring System Configurations

DMTD System Configuration	Input Connections		Output Usage	Remarks
	Section A	Section B		
Standard	A = Ref clock 2 = Meas 1 A1 to Input 1	3= Meas 2 A2 to Input 3 B splitter NC	TIC A = 1 vs Ref TIC B = 2 vs Ref	Two meas clocks measured against Ref clock using standard DMTD methodology.
Correlation	A = Ref clock A1 to Input 1 A2 to Input 3	B=Meas Clock B3 to Input 2 B4 to Input 4	TIC A = Ref TIC B = Meas Use Cross ADEV	Ref and meas clocks compared with sections A and B. Cross ADEV cancels uncorrelated noise.
Coherent A	A = Source A1 to Input 1 A2 to Input 2	Optional	TIC A = System Noise	Coherent inputs to measure system noise. Section B can be used in same way.
Cross Coherent	A = Source A1 to Input 1 A2 to Input	B = Source B3 to Input 2 B4 to Input 4	TIC A = Meas 1 TIC B = Meas 2 Use Cross ADEV	Coherent inputs from external splitter to measure cross correlation system noise.
In the case of a 1-section measurement at 10 MHz, the B power splitter can be used to drive the Reference input and A section power splitter from a single 10 MHz source.				

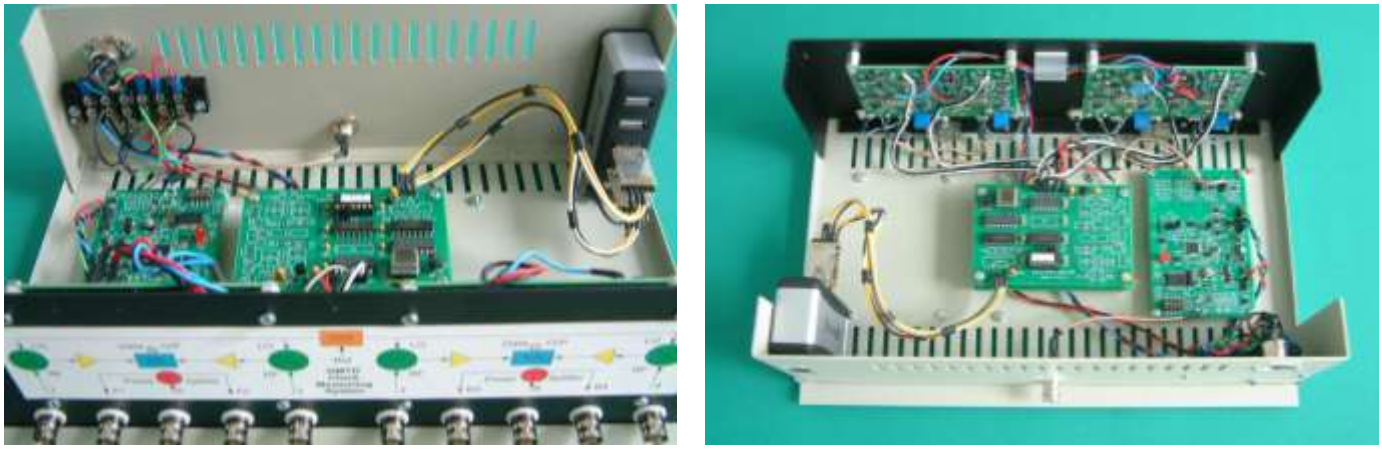


Figure 5. Photographs of the Small DMTD Clock Measuring System

Expanded DMTD System

The basic DMTD clock measuring system may be expanded with a 3rd TIC whose start input is connected to the ZCD of mixer 1 and whose stop input is connected to the ZCD of mixer 3 as shown in Figure 6.

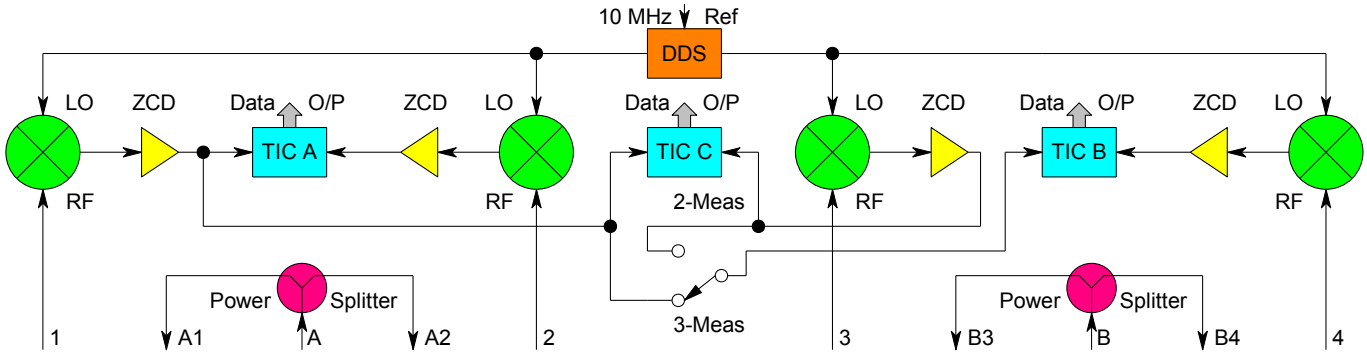


Figure 6. Expanded DMTD Clock Measuring System

In this arrangement, the 2-meas coherent configuration with separate A and B sources can use TIC C as an optional incoherent output. In the 3-meas arrangement with the TIC B start input also connected to the ZCD of mixer 1, the system can be used to measure three clocks against the Input 1 reference, a configuration well-suited for 3-cornered hat intercomparisons.

DMTD Clock Measuring Systems

A DMTD clock measuring system combines the heterodyne technique of resolution enhancement with a time interval counter to measure the relative phase of the beat signals from a pair of mixers driven from a common offset reference. It is one of the most precise ways to compare clocks all having the same nominal frequency. Its advantages include high resolution, low noise, phase data, no fixed reference channel and cancellation of offset reference noise and inaccuracy, while its disadvantages include complexity and operation at a single carrier frequency.

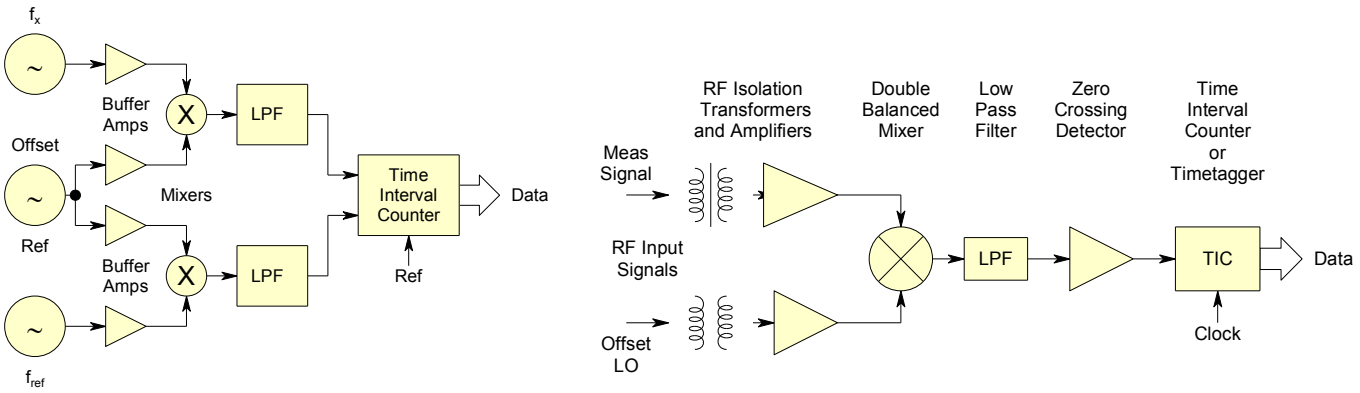


Figure 7. Block Diagrams of a DMTD Clock Measuring System

The DMTD system can be expanded to multiple channels by adding additional buffer amplifiers and mixers, and time tagging the zero-crossings of the beat notes for each channel, this arrangement allows any two of the clocks to be intercompared. The offset reference need not be coherent, nor must it have particularly low noise or high accuracy, because its effect cancels out in the overall measurement process. For best cancellation, the zero-crossings should be coincident or interpolated to a common epoch. Additional counters can be used to count the whole beat note cycles to eliminate their ambiguity, or the zero-crossings can simply be time tagged. The measuring system resolution is determined by the time interval counter or time tagging hardware, and the mixer heterodyne factor. For example, if two 5 MHz sources are mixed against a common 5 MHz - 10 Hz offset oscillator (providing a $5x10^6/10 = 5x10^5$ heterodyne factor), and the beat note is timetagged with a resolution of 100 nsec (10 MHz clock), the measuring overall system resolution is $10^{-7}/5x10^5 = 0.2$ psec.

Multichannel DMTD clock measuring systems have been utilized by leading national and commercial metrology laboratories for a number of years [1-5, 18-20]. An early commercial version is described in Reference [3], a newer technique is described in Reference [8], and the Timing Solutions Corporation TS-3020 is an example of such a system [6]. The Stable32 software [11] has capabilities for reading the data files created by a TS-3020 system, allowing clock records to be conveniently processed.

The RF signals are isolated by RF transformers to avoid ground loops, and by isolation amplifiers to provide good input cable termination and reverse isolation for mixer products. It is important that those components have low phase sensitivity to temperature variations. The mixer is followed by a low pass filter to separate the audio beat signal from the RF components. The most critical component is the zero crossing detector or comparator that converts the analog beat signal into a digital waveform. It must have low noise and offset, and high speed so that the relatively slow beat signal is converted to a fast switching signal with low jitter at its exact zero crossing, and without crosstalk between adjacent channels [16].

The zero crossing detector output becomes one input of a time interval counter, or is timetagged by a digitizer with respect to an external system clock. The former is most commonly used for a simple heterodyne system, while the latter is generally used in a multi-channel DMTD system. Because of the large heterodyne factor that is normally used (e.g., 10^6 for a 10 Hz beat note with 10 MHz signals), high measurement resolution does not require particularly fast time measurements (e.g., 0.1 psec overall resolution for a 10 MHz clock).

It is important to understand the potential vulnerability of a clock data acquisition system to interfering signals such as power line ripple. Signals at frequencies higher than one-half the sampling rate (e.g. 5 Hz for a 10 Hz beat note) are aliased and appear in the data as interference at lower frequencies. The system does not, and, as a practical matter, cannot have, low pass filtration to avoid such aliasing. Hence the importance of the RF isolation transformers and other precautions to avoid contamination by interfering signals. One should be alert to strange results, such as oscillations in an Allan deviation plot, which can be a sign of an aliasing problem. A higher beat frequency and sampling rate, perhaps followed by digital low pass filtration and decimation, is another way to reduce those problems, at the expense of lower resolution or the need for a higher performance time digitizer. Satisfactory results are usually obtained, as long as one remains aware of the possibility of aliasing difficulties.

The Small DMTD Clock Measuring System

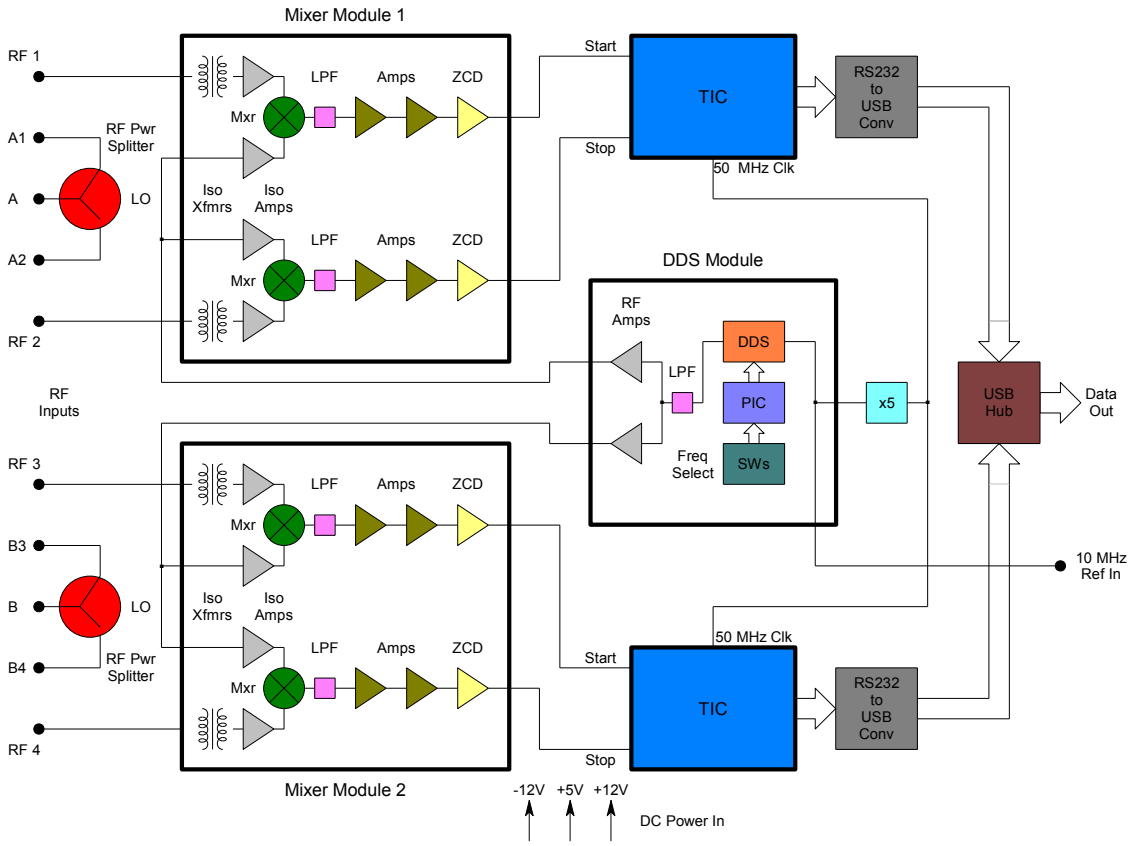
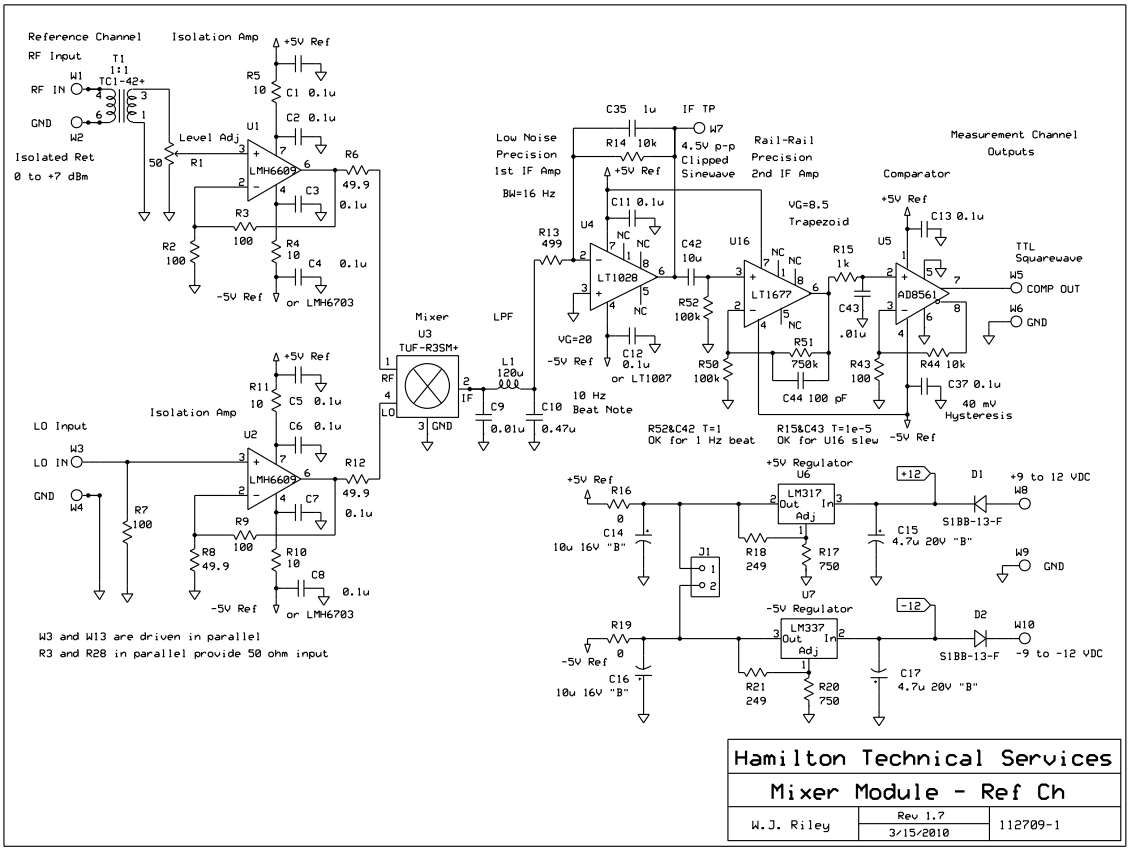


Figure 8. Block Diagram of the Small DMTD Clock Measuring System

Mixer Module

The mixer module of the Small DMTD system follows the general approach described in Reference 16 and 23, with a signal path that progresses from a low noise narrow bandwidth low slew rate input stage to a fast output stage zero crossing detector. Its distinguishing features are AC coupling to suppress the DC offset TC of the mixer diodes and the use of a high speed comparator as the last stage.



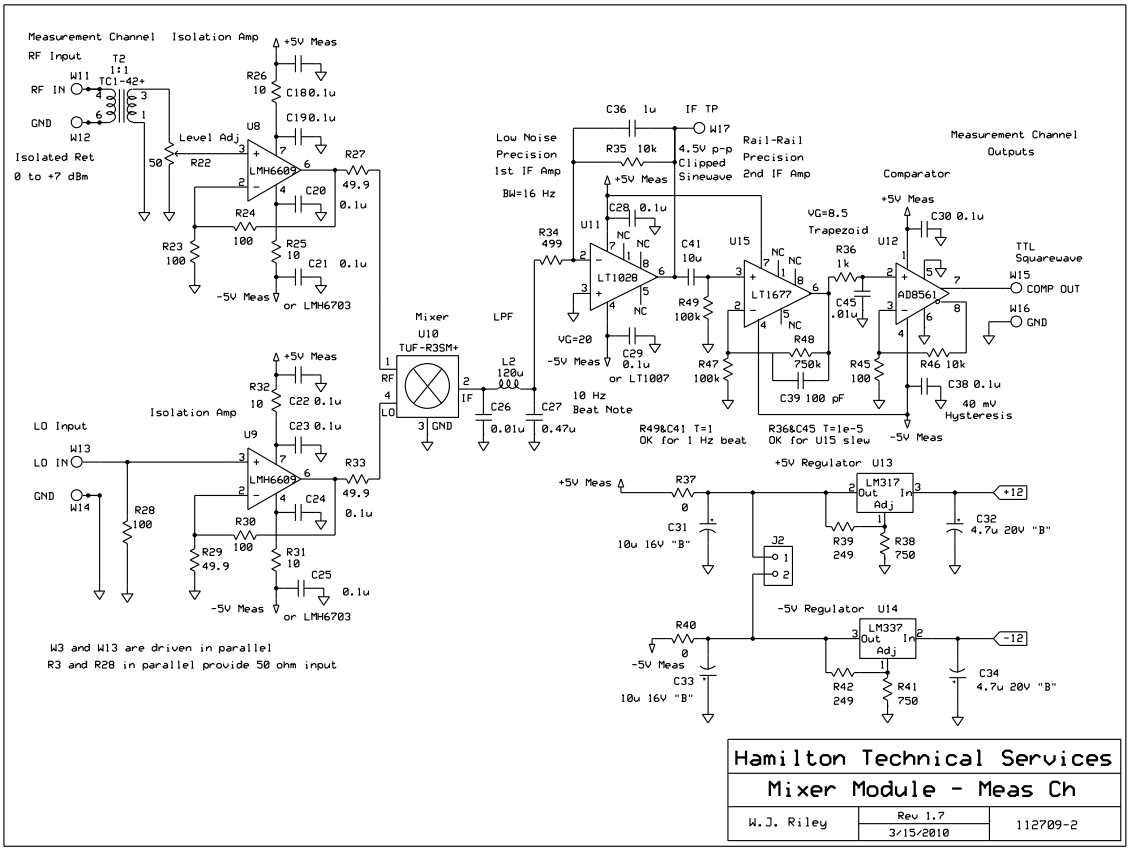


Figure 9. Mixer Module Schematic

The circuit schematic and board layout of the experimental Small DMTD Mixer Module are shown in Figures 9 and 10.

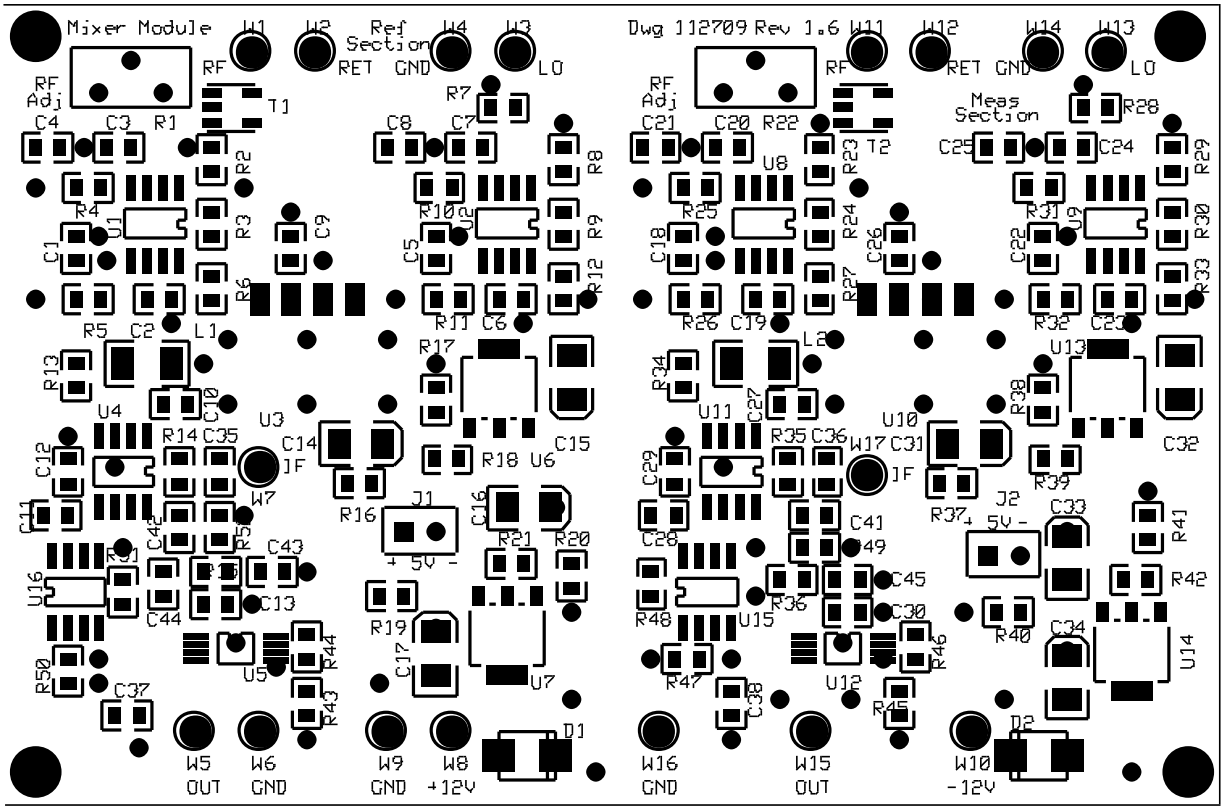
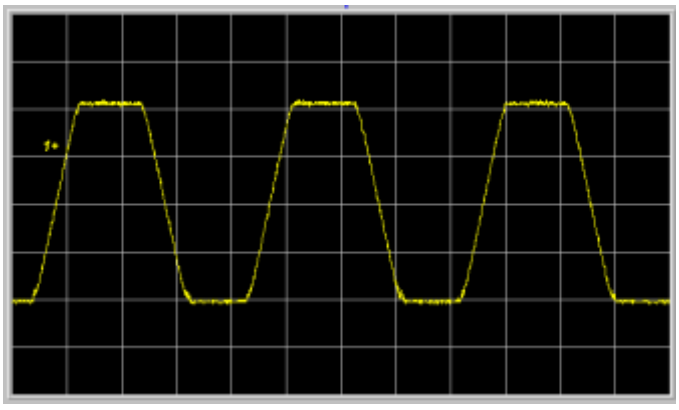
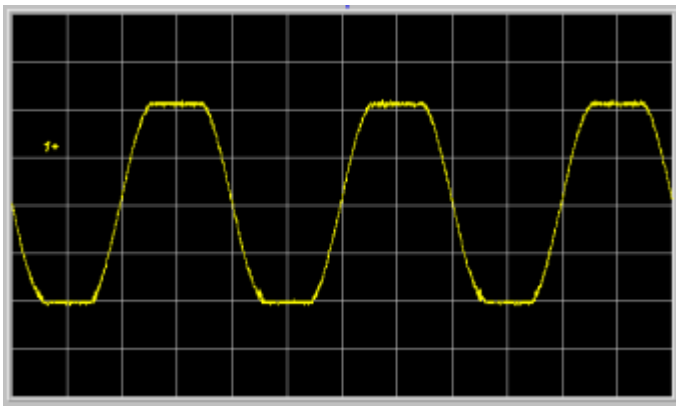


Figure 10. Mixer Module Board Layout

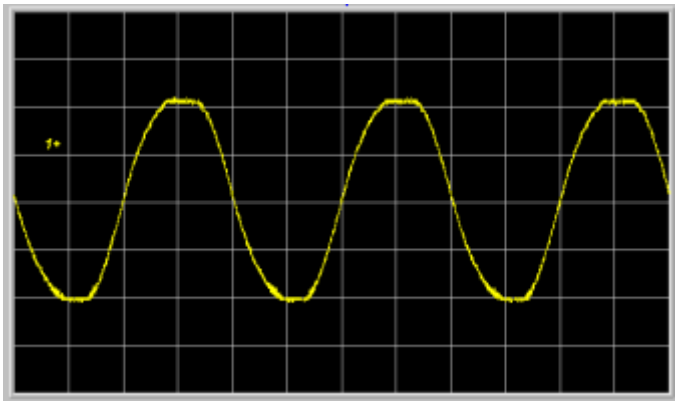
The waveforms at the IF test point at the output of the first IF amplifier are shown in Figure 11 for beat frequencies of 1, 5, 10 and 100 Hz with an RF input level of +3 dBm, the RF level adjustment set to maximum, and a first IF amplifier voltage gain of 20 and a bandwidth of 16 Hz. Figure 12 shows the IF test point waveforms at 10 Hz at RF inputs of 0 and +7 dBm, and Figure 13 shows the waveforms at the output of the IF amplifier (the input to the comparator) at those RF levels.



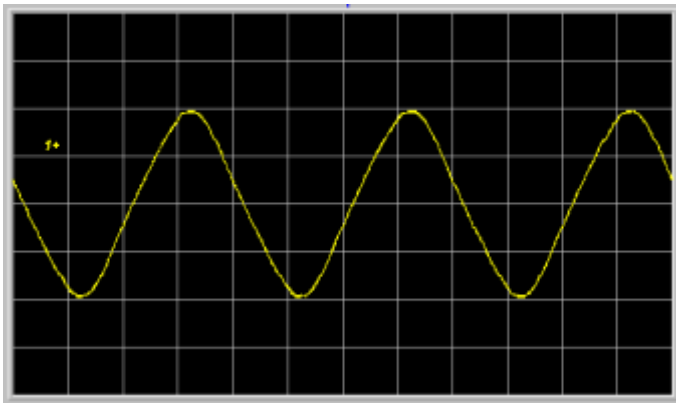
f=1 Hz , X=250 ms/div, Y=2 V/div, S=36 V/s



f=5 Hz , X=50 ms/div, Y= 2 V/div, S=160 V/s

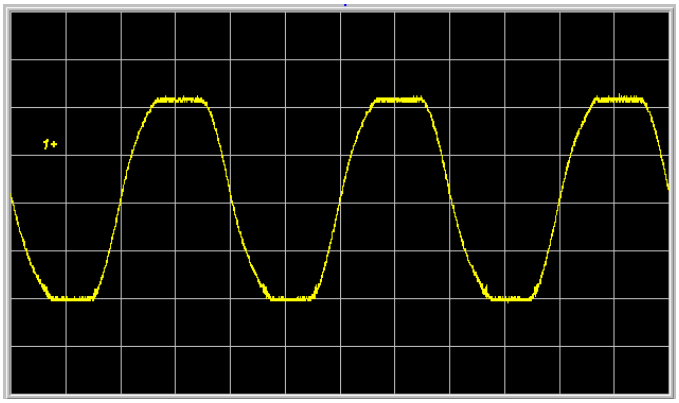


f=10 Hz , X=25 ms/div, Y=2 V/div, S=320 V/s

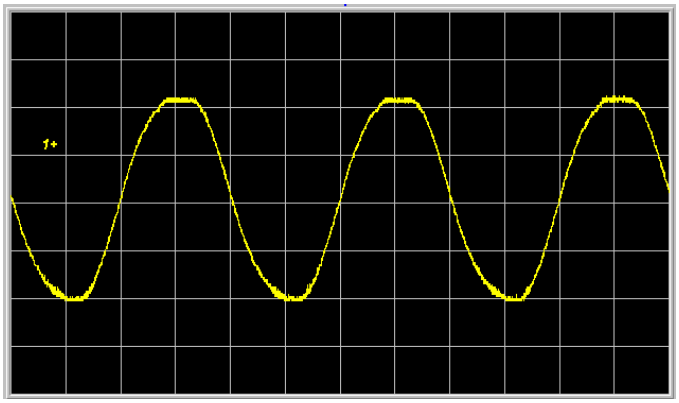


f=100 Hz , X=2.5 ms/div, Y=0.5 V/div, S=530 V/s

Figure 11. IF Test Point Waveforms at RF=+3 dBm, IF Gain=Max, VG=20, BW=16 Hz

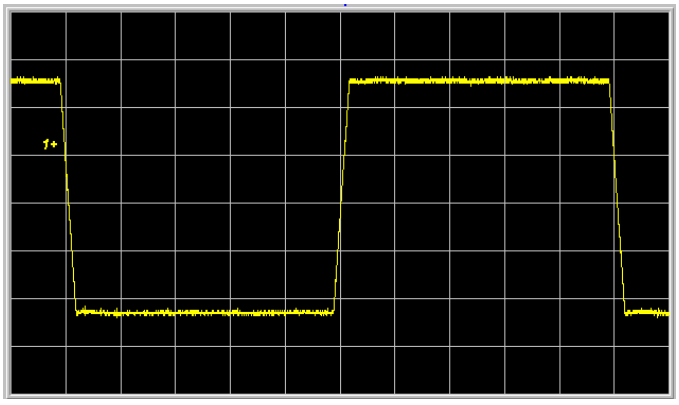


RF = +7 dBm, X = 25 ms/div, Y = 2 V/div

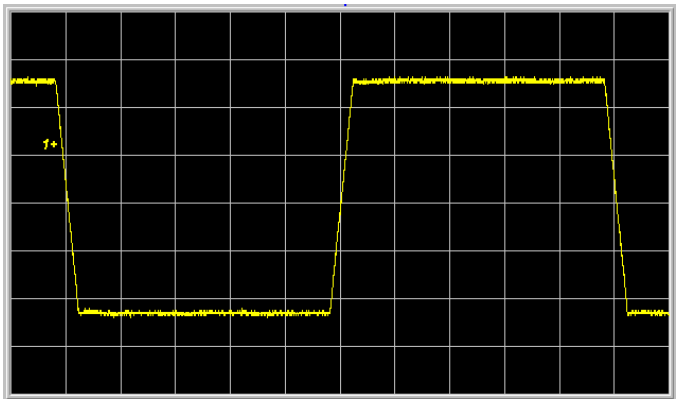


RF = 0 dBm, X = 25 ms/div, Y = 2 V/div

Figure 12. IF Test Point Waveforms at f=10 Hz, IF Gain=Max, VG=20, BW=16 Hz



RF=+7 dBm, X=10 ms/div, Y=2 V/div, S=3.3V/ms



RF=0 dBm, X=10 ms/div, Y=2 V/div, S=2.5 V/ms

Figure 13. IF Amplifier Output Waveforms at f=10 Hz, IF Gain=Max, Overall VG=170

● Time Interval Counter Module

The Small DMTD system uses a version of the PICTIC time interval counter designed by Richard McCorkle [21]. In particular, this application uses a 50 MHz clock prescaler PICTIC without an analog interpolator and with a higher serial communications rate. A block diagram of this PICTIC is shown in Figure 14. Detailed design, schematic, parts list, board layout and assembly code information for the PICTIC is available in Reference 21.

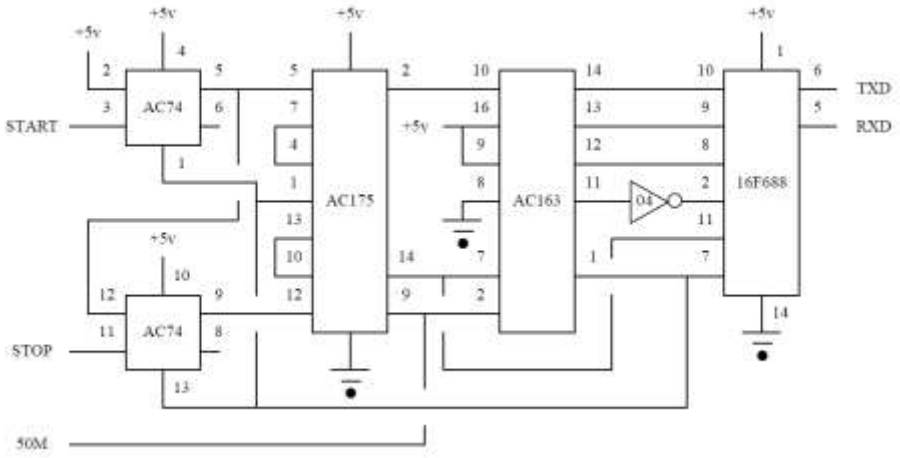


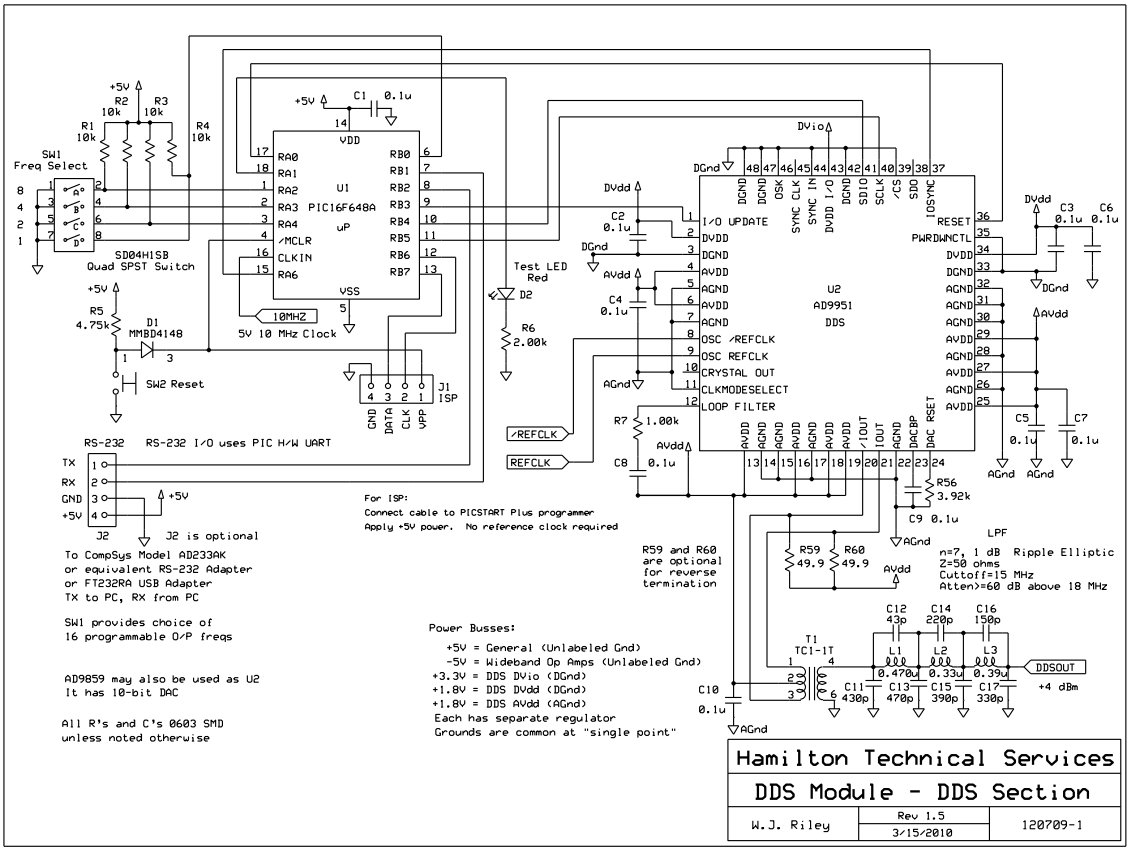
Figure 14. Block Diagram of PICTIC Time Interval Counter

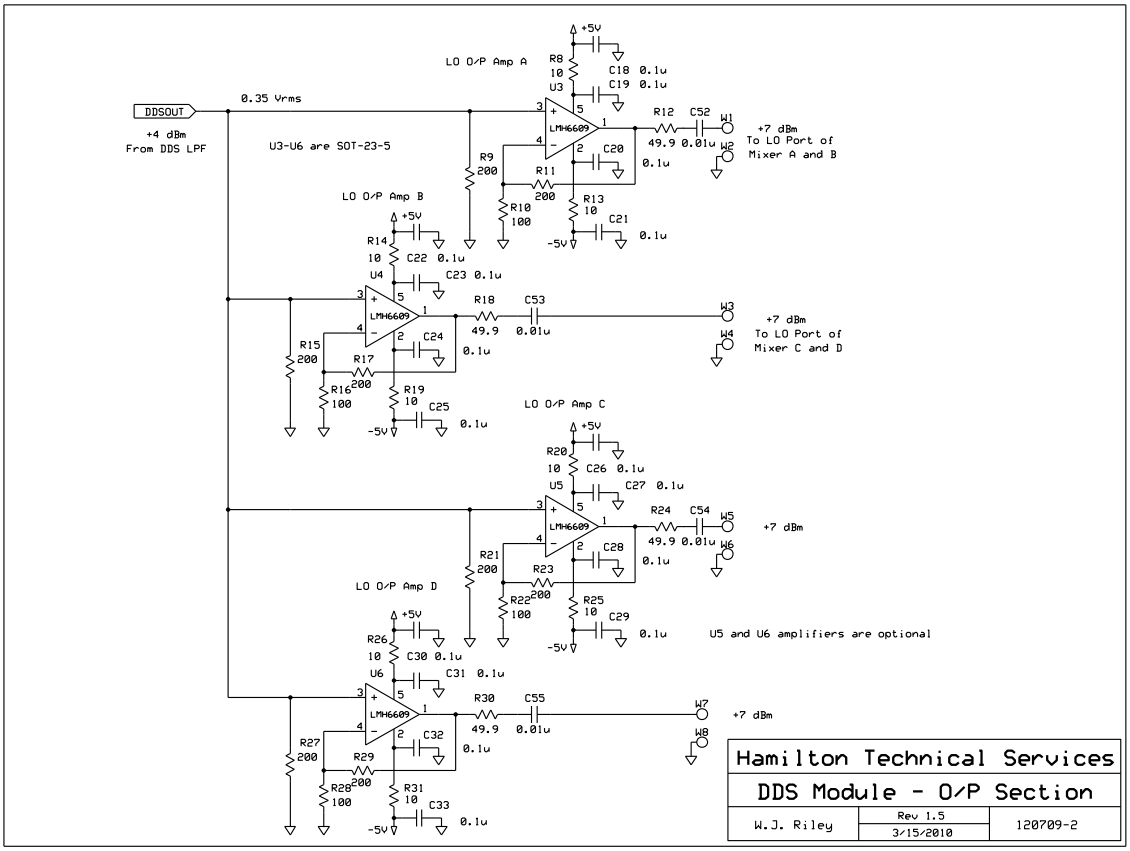
Several approaches were investigated for the 50 MHz PICTIC clock source, including free-running 50 MHz XOs, 100 MHz OCXOs divided to 50 MHz, a phase-locked 100 MHz OCVCXO divided to 50 MHzs and a x5 harmonic multiplier from 10 MHz, the latter chosen as the most practical coherent choice. Inaccuracy of the TIC clock affects the measurement scale factor, deleveraged by the system heterodyne factor.

● DDS Module

The DDS module provides the offset LO signal for the Small DMTD clock measuring system. It comprises …

A schematic diagram for this module is shown in Figure 15. This schematic incorporates the changes made during evaluation of the first experimental version, including the addition of a x5 TIC clock multiplier. Only two of the four O/P amplifiers are required, and the 10 MHz reference O/P amplifier is also not required.


SW1
Freq Select
SD04H1SB
Quad SPST Switch
R1 10k
R2 10k
R3 10k
R4 10k
+5V
U1
PIC16F648A
uP
VDD
VSS
/MCLR
CLKIN
RA0
RA1
RA2
RA3
RA4
RA6
RB0
RB1
RB2
RB3
RB4
RB5
RB6
RB7
C1 0.1u
10MHZ
5V 10 MHz Clock
R5 4.75k
D1 MMBD4148
SW2 Reset
J1 ISP
GND DATA CLK VPP
Test LED Red
D2
R6 2.00k
U2
AD9951
DDS
DVio
DGnd
DVdd
AVdd
AGnd
I/O UPDATE
DVDD
DGND
AVDD
AGND
OSC /REFCLK
OSC REFCLK
CRYSTAL OUT
CLKMODESELECT
LOOP FILTER
SYNC CLK
SYNC IN
DVDD I/O
SDIO
SCLK
/CS
SDO
IOSYNC
RESET
PWRDWNCTL
DACBP
DAC RSET
IOUT
/IOUT
C2 0.1u
C3 0.1u
C4 0.1u
C5 0.1u
C6 0.1u
C7 0.1u
C8 0.1u
C9 0.1u
R7 1.00k
R56 3.92k
/REFCLK
REFCLK
RS-232
RS-232 I/O uses PIC H/W UART
TX
RX
GND
+5V
J2
J2 is optional
To CompSys Model AD233AK
or equivalent RS-232 Adapter
or FT232RA USB Adapter
TX to PC, RX from PC
SW1 provides choice of
16 programmable O/P freqs
AD9859 may also be used as U2
It has 10-bit DAC
All R's and C's 0603 SMD
unless noted otherwise
For ISP:
Connect cable to PICSTART Plus programmer
Apply +5V power. No reference clock required
R59 and R60
are optional
for reverse
termination
R59 49.9
R60 49.9
LPF
n=7, 1 dB Ripple Elliptic
Z=50 ohms
Cuttoff=15 MHz
Atten>=60 dB above 18 MHz
C12 43p
C14 220p
C16 150p
T1
TC1-1T
L1 0.470u
L2 0.33u
L3 0.39u
C11 430p
C13 470p
C15 390p
C17 330p
C10 0.1u
DDSOUT
+4 dBm
Power Busses:
+5V = General (Unlabeled Gnd)
-5V = Wideband Op Amps (Unlabeled Gnd)
+3.3V = DDS DVio (DGnd)
+1.8V = DDS DVdd (DGnd)
+1.8V = DDS AVdd (AGnd)
Each has separate regulator
Grounds are common at "single point"
Hamilton Technical Services
DDS Module - DDS Section
W.J. Riley
Rev 1.5
3/15/2010
120709-1


LO O/P Amp A
LO O/P Amp B
LO O/P Amp C
LO O/P Amp D
DDSOUT
+4 dBm
From DDS LPF
0.35 Vrms
U3-U6 are SOT-23-5
LMH6609
+7 dBm
To LO Port of
Mixer A and B
To LO Port of
Mixer C and D
U5 and U6 amplifiers are optional
Hamilton Technical Services
DDS Module - O/P Section
W.J. Riley
Rev 1.5
3/15/2010
120709-2

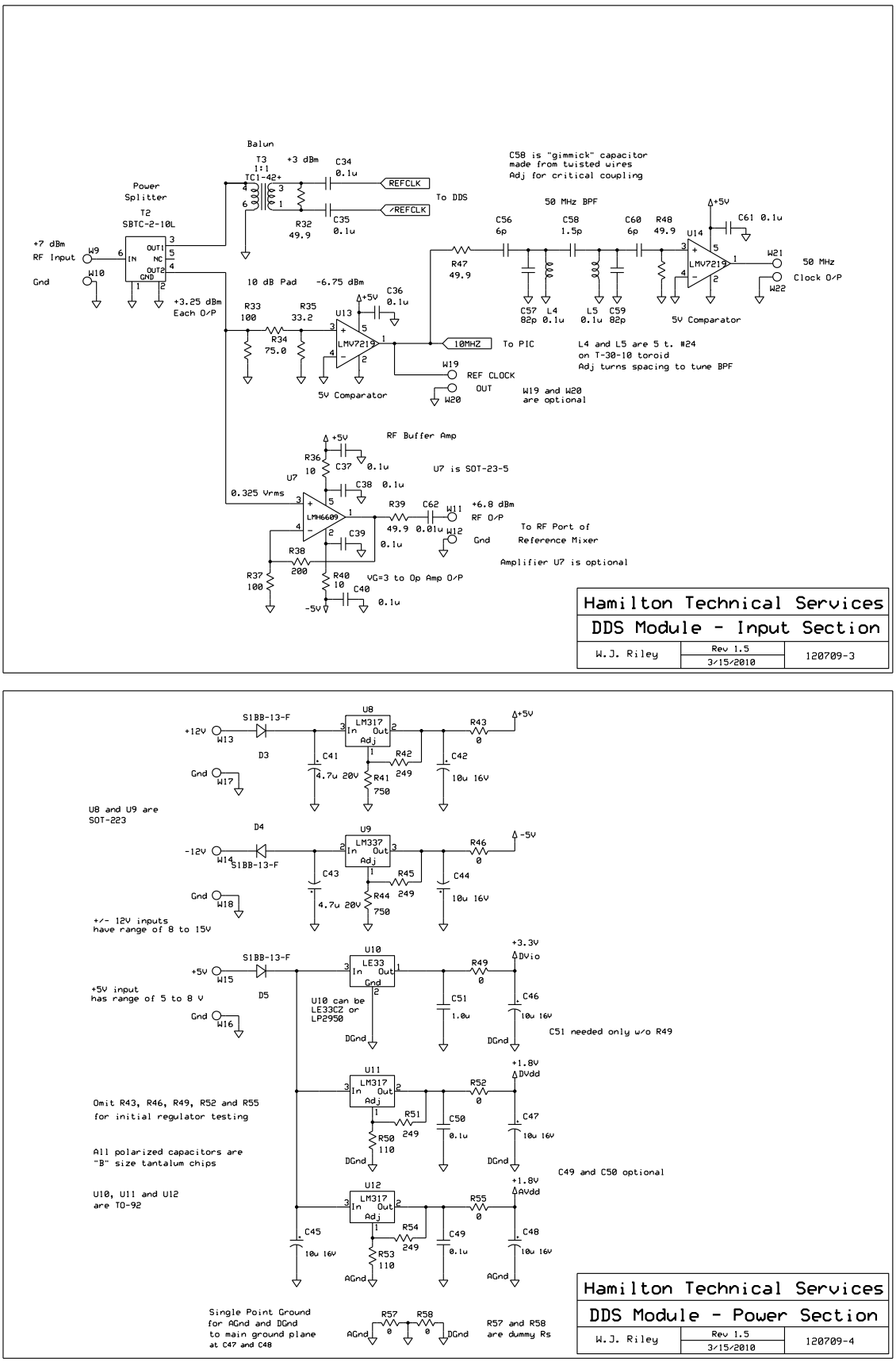


Figure 15. DDS Module Schematic

The DDS module is pre-programmed with 16 frequency settings selectable via an on-board DIP switch, as shown in Table 2. These choices provide frequency offsets of 1, 5, 10 and 100 Hz for four RF frequencies associated with GPS satellite atomic clocks.

Table 2. Standard Offset LO DDS Settings

Switch Setting		RF Frequency	Freq Offset	DDS Word	DMTD Resolution, Δf/f
Decimal	Binary	MHz	Hz	Hex	For 50 MHz TIC Clock
00	0000	5	1	0AAAAACE	4.000000e-15
01	0001		5	0AAAAB5D	2.000000e-14
02	0010		10	0AAAAC10	4.000000e-14
03	0011		100	0AAAB8A5	4.000000e-13
04	0100	10	1	15555579	2.000000e-15
05	0101		5	15555608	1.000000e-14
06	0110		10	155556BB	2.000000e-14
07	0111		100	15556350	2.000000e-13
08	1000	10.23	1	15D2F1CD	1.955034e-15
09	1001		5	15D2F25C	9.775171e-15
10	1010		10	15D2F30F	1.955034e-14
11	1011		100	15D2FFA5	1.955034e-13
12	1100	13.40134393	1	1C96EBD2	1.492388e-15
13	1101		5	1C96EC61	7.461938e-15
14	1110		10	1C96ED14	1.492388e-14
15	1111		100	1C96F9A9	1.492388e-13

Other frequencies can be substituted in the DDS module PIC firmware, and it has provisions (currently unimplemented) to enter frequency settings via a user interface through the same USB hub as used for the clock data. As presently configured with a 16 Hz IF bandwidth, the 100 Hz beat frequency is not well-supported, nor does the DMTDComm program work at that rate with its plotting features, although the raw DMTD data stream can be captured with Windows HyperTerminal for subsequent scaling and processing. Similarly, the IF bandwidth is unnecessarily wide, and the 0.16 Hz AC coupling in the IF amplifier is not ideal, for a 1 Hz beat frequency.

The board layout of the experimental Small DMTD DDS Module is shown in Figure 16.

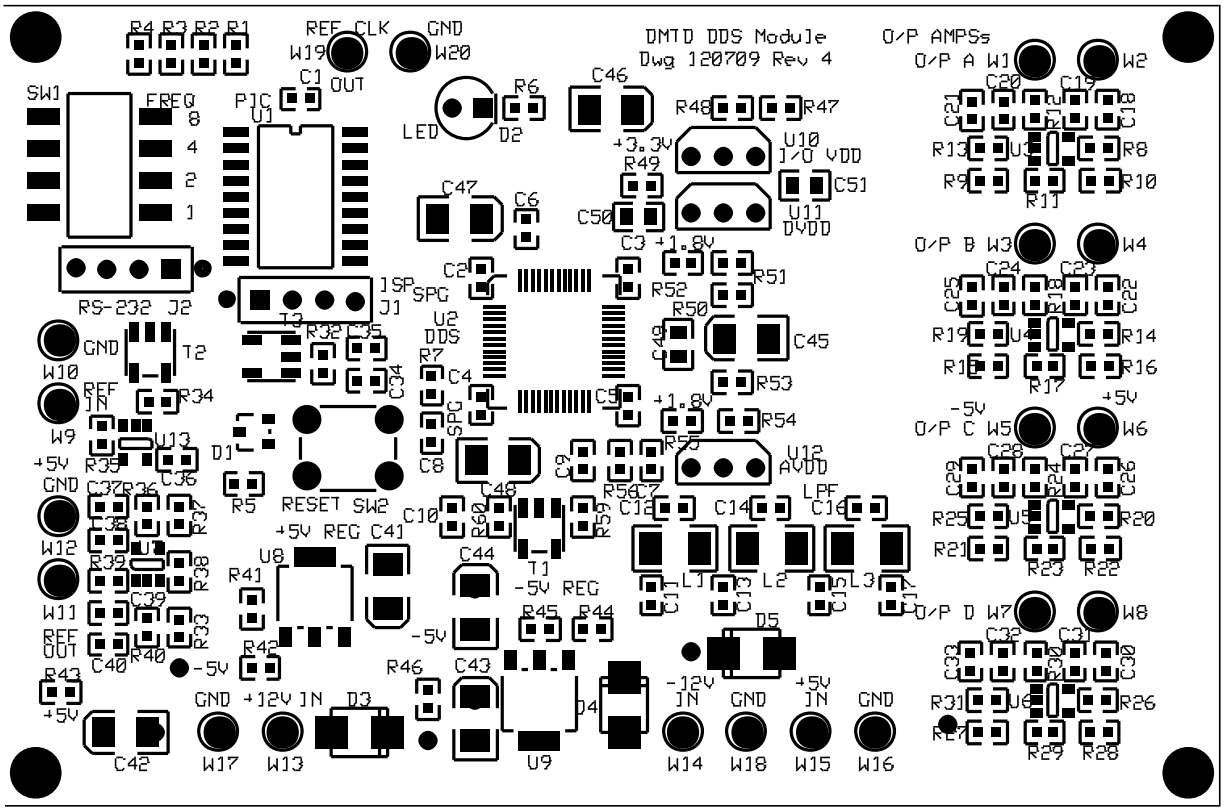


Figure 16. DDS Module Board Layout

- **LO Distribution**

The DDS module has provisions for four isolated 50 Ω outputs to drive the LO inputs of the two dual mixer module via separate coaxial cables, but, to maintain best coherency, a single DDS output is used for each mixer module. The two LO inputs of each mixer module have paralleled 100 Ω termination resistors connected with a short length of ≈100 Ω twisted pair.

- **TIC Clock**

The 50 MHz time interval counter clock should be coherent with the offset LO reference to avoid beats and other interference effects. That is accomplished from the 10 MHz reference squarewave by a passive x5 harmonic multiplier implemented by a 2-pole bandpass filter and high-speed comparator. Experiments conducted with a PIC clock derived from a free-running 100 MHz OCVCXO showed unexpectedly large (> $pp10^{10}$) fluctuations as the oscillator was tuned slightly away from zero-beat that were dependent on grounding and lead dress. It is convenient to provide a switch to turn off and on the TIP clock as a way to start and stop the measurements on all channels simultaneously.

● USB Data Interface

Data from the two TICs (three for an expanded system) are converted from TTL RS-232 to USB format by FTDI FT232R chips and combined in a USB hub inside the Small DMTD box. The same method can be used to communicate with the optional DDS module user interface. At the PC end, the USB connection is treated as a virtual COM port. The system uses 57600 baud, the highest rate supportable by the PICTIC processor.

Although TIC data is taken simultaneously for two coherent RF channels, these data are transferred via the serial USB interface sequentially and therefore obtain slightly different timetags. That difference is simply ignored for the case of the two data sets of a cross-correlation measurement.

● DMTDComm Software

Operation of the Small DMTD clock measuring system is supported by the DMTDComm PC program that runs under Microsoft Windows®. This program configures and controls the Small DMTD system, displays the data stream as a list or plot of the phase or frequency, and captures the data to a disk file for analysis by Stable32. Multiple instances of DMTDComm can be launched to handle several Small DMTD measurement sections. The DMTDComm Main and Configure screens are shown in Figures 17 and 18 respectively.

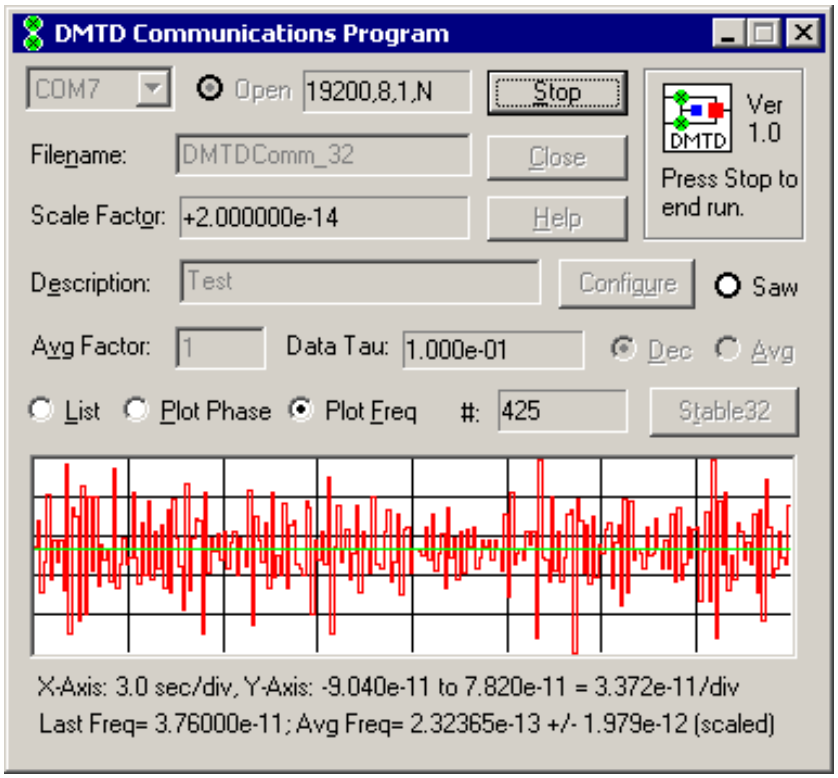


Figure 17. DMTD Main Screen

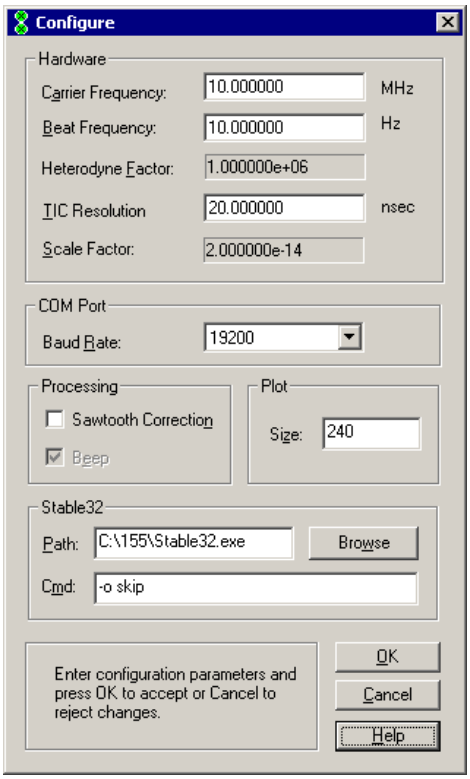


Figure 18. DMTD Configure Screen

The phase and frequency plots and their annotations provide immediate feedback about the measurement results. The former can be used to assist in adjusting the relative phase of the RF inputs. During a cross-correlation coherent test, the latter plot for two sections will be highly correlated.

Data File Format

The DMTDComm program writes a Stable32-compatible data file, as shown in the example of Figure 19. The file header includes lines indicating the Small DMTD system and the measurement tau. The first column is the MJD (derived from the local PC clock) when the data was written to the file (with a resolution of about 0.86 ms), and the second column is the phase reading in seconds (with a resolution exceeding that of the PICTIC).

```
Small DMTD Clock Measuring System
Left Section
Tau: 1.000e-01
MJD              Phase, seconds
55267.54928600 1.412200000000000e-10
55267.54928715 1.412400000000000e-10
55267.54928819 1.411800000000000e-10
55267.54928936 1.412200000000000e-10
55267.54929064 1.412400000000000e-10
55267.54929179 1.411400000000000e-10
```

Figure 19. DMTDComm Data Format

Decimation and Averaging

The DMTDComm program supports phase decimation and averaging. Decimation simply discards every nth phase data point. It is equivalent to frequency averaging, and is appropriate to reduce the amount of data when information at the shorter tau is not required. Phase averaging also reduces the size of the data file at the expense of losing information at shorter tau, but it also reduces the noise and changes the statistical properties of the data. Phase averaging is therefore seldom done and, if done, must be used with caution. Stability plots of decimated and averaged phase data from two portions of the same coherent run are shown in Figures 20 and 21. Both data sets have flicker PM noise with $\alpha \approx +1.2$ at $\tau = 1$ second but the ADEV for the averaged data is x3.0 ($\approx \sqrt{10}$) lower.

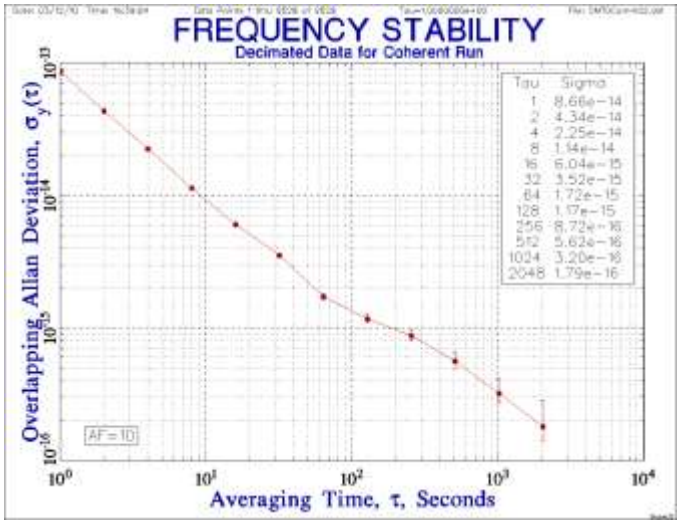


Figure 20. Stability Plot of Decimated Phase Data

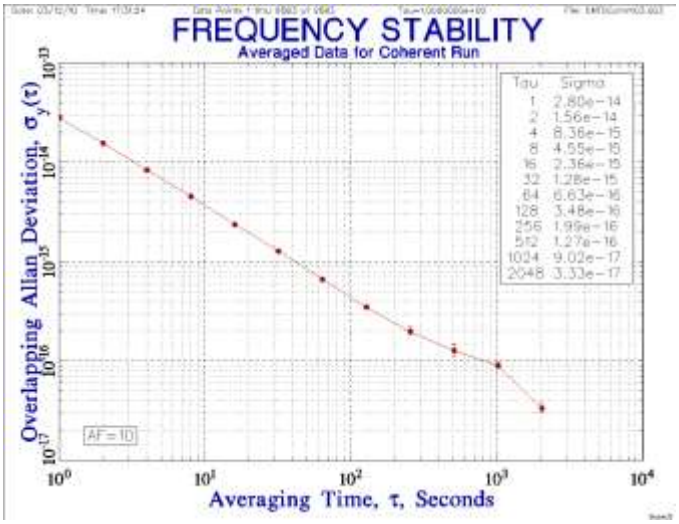


Figure 21. Stability Plot of Averaged Phase Data

Coherent Noise Floor

The noise floor of the Small DMTD system can be measured by applying the same source coherently to both RF inputs of a DMTD section. This can be done most easily by means of an internal RF power splitter. An example of a coherent noise floor test is shown in Figures 22-25 below.

Figure 22. Coherent Phase Data

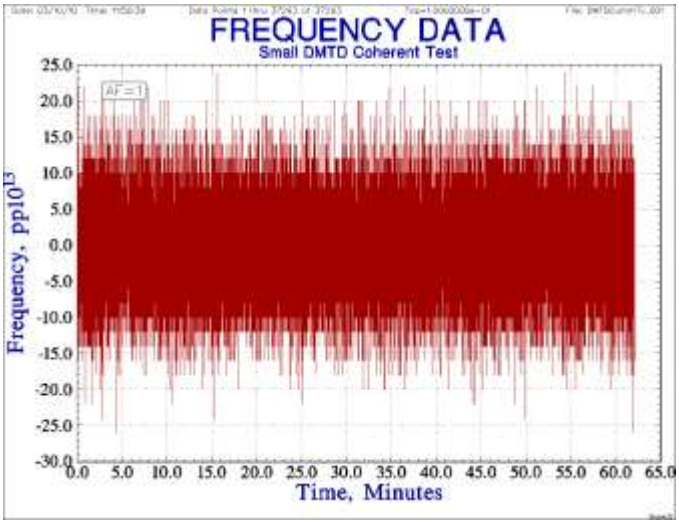


Figure 23. Coherent Frequency Data

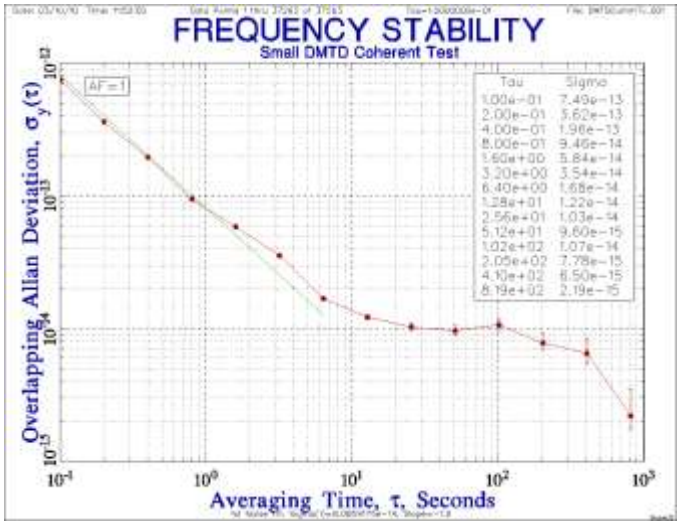


Figure 24. Coherent Stability Noise Floor

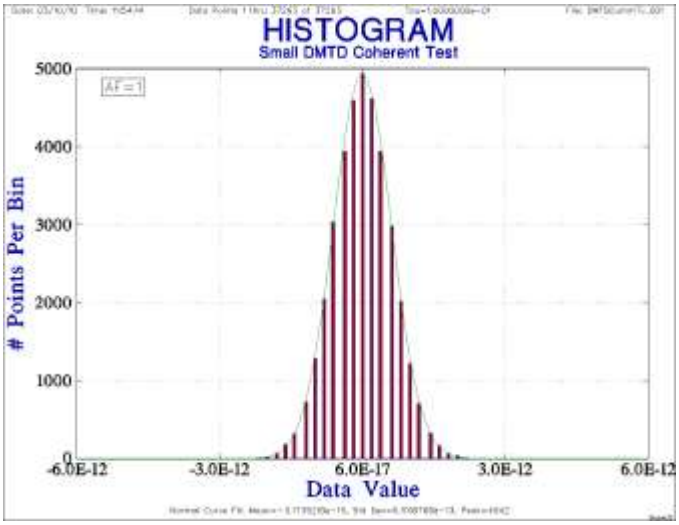


Figure 25. Histogram of Frequency Data

The 1-second Small DMTD coherent noise floor is about x100 lower than the noise of the rubidium oscillator used as the common source (say $1x10^{-11}$ at 1-second), and is most likely limited by the degree of coherence rather than the noise of the measuring system. The most important factor determining the noise floor appears to be the relative delay between the two RF inputs rather than any aspect of the measuring system itself. When this phase difference is large, cancellation of the RF source noise is poor and one sees white FM noise at a higher level than when the phase difference is small and one sees a lower level of white PM noise for the DMTD system.

Coherent tests can be done at the other standard RF frequencies of 5, 10.23 and 13.40134393 MHz by using a high-resolution DDS at both RF inputs. But when a coherently-referenced DDS was used at 10 MHz as one of the RF inputs, it was found that the noise level was an order-of-magnitude higher even if its relative phase was adjusted close to zero, perhaps because of its internal clock multiplier.

Coherent Cross-Correlation Noise Floor

The coherent cross-correlation noise floor can be measured by taking simultaneous coherent data with DMTD sections, starting and stopping the measurements with a TIC clock switch. Results of a longer coherent cross-correlation run are shown in Figures 26-34 below. The nominal phase difference of each section was adjusted to a small value of ≈ 0.2 ns for good source noise cancellation. The measuring system noise had a $\alpha \approx +1.5$ at $\tau = 0.1$ second, between white and flicker PM. The 2×10^{-14}/second quantization level is visible in both the phase and frequency data plots, and most clearly in the frequency histograms, which are normally-distributed.

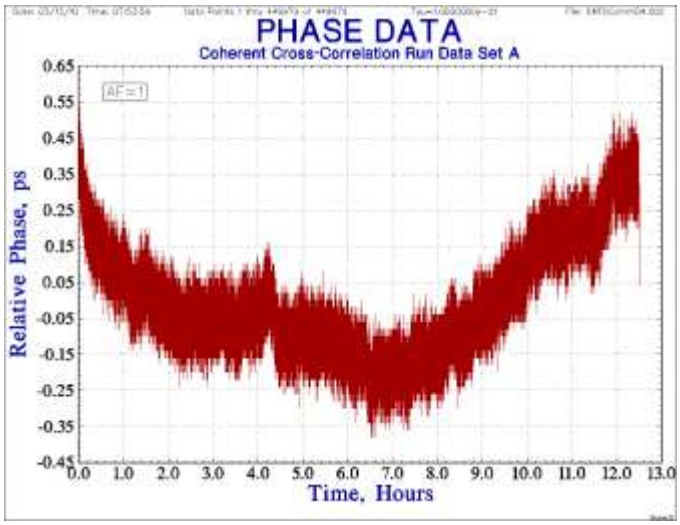


Figure 26. Phase Record

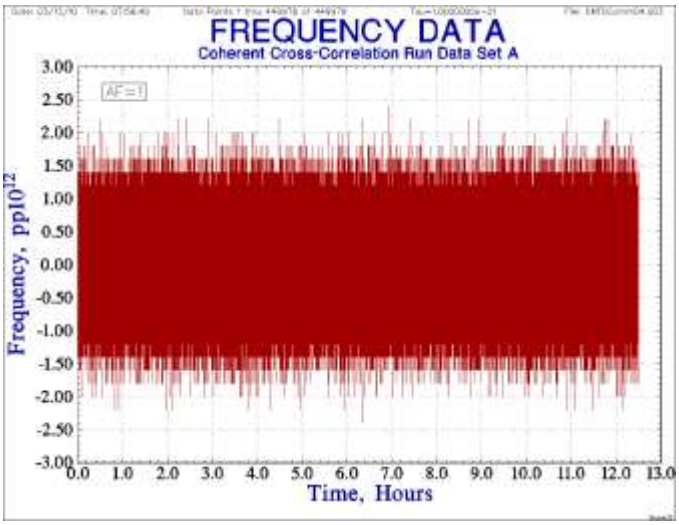


Figure 27. Frequency Record

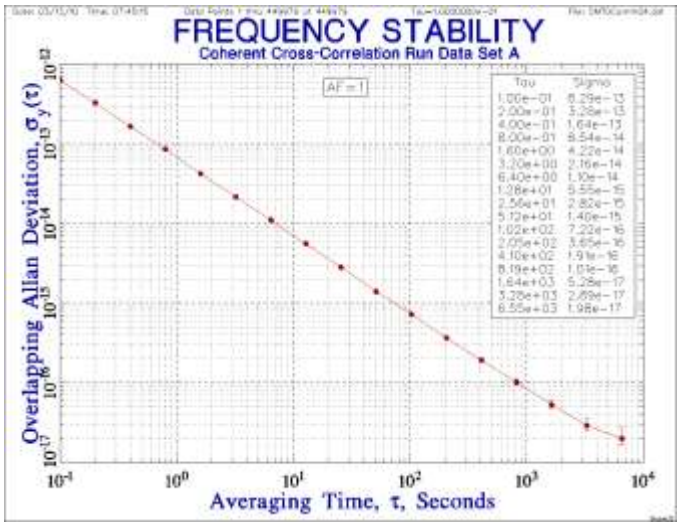


Figure 28. Frequency Stability

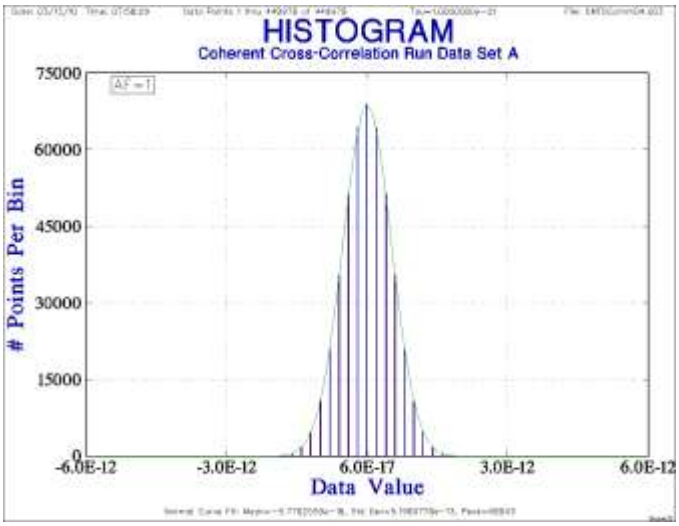


Figure 29. Frequency Histogram

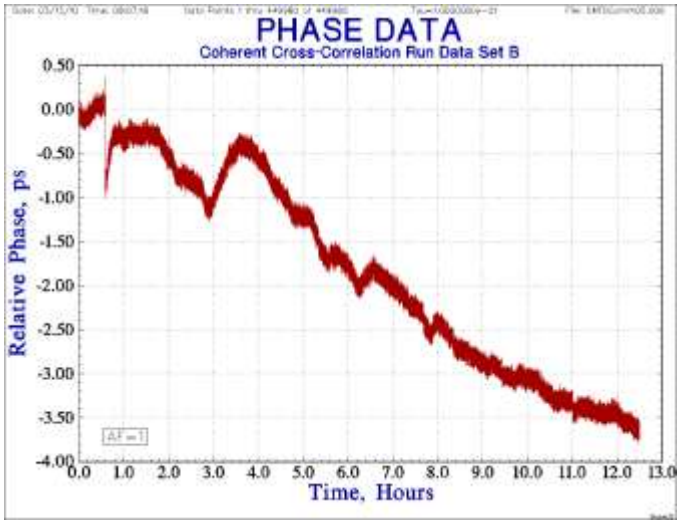


Figure 30. Phase Record

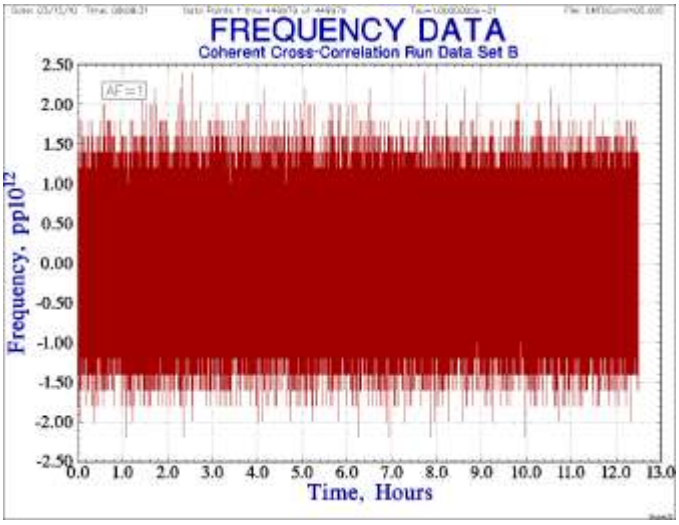


Figure 31. Frequency Record

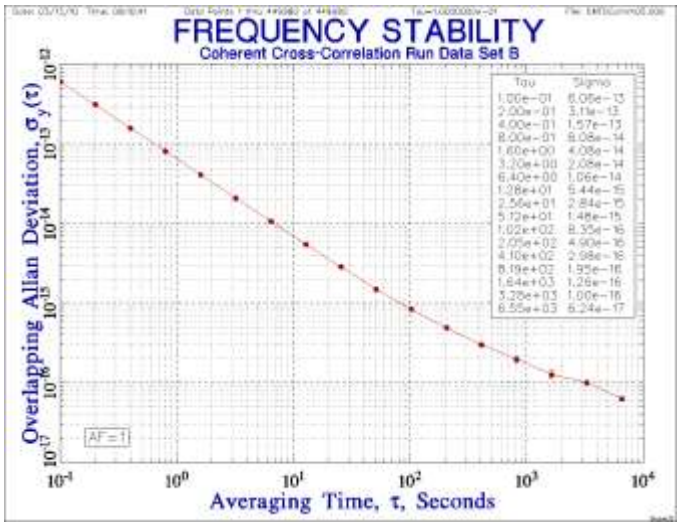


Figure 32. Frequency Stability

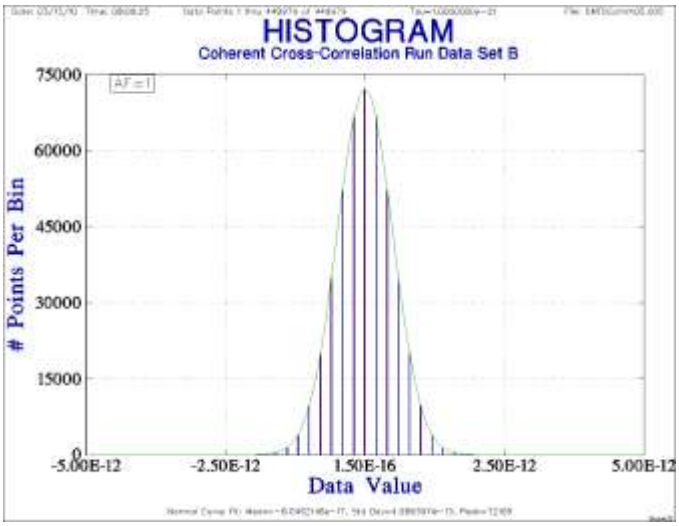


Figure 33. Frequency Histogram

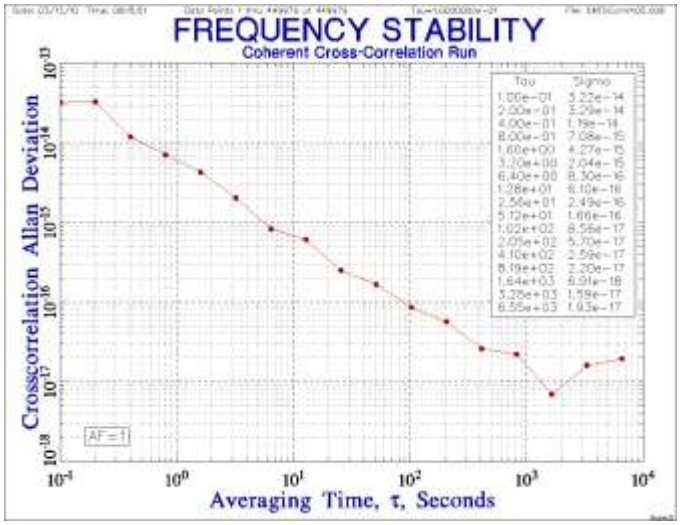


Figure 34. Cross-Correlation Frequency Stability

These data produced a 1-second cross-correlation ADEV of about 6.0×10^{-15}, as shown in the #ADEV stability plot of Figure 34. Compared with the individual 1-second stabilities of about 6.5×10^{-14}, the cross-correlation technique improved the noise floor by a factor of about x10.

- **LO Offsets**

The standard Small DMTD LO frequency offset options are 1, 5, 10 and 100 Hz, providing resolutions of 2e-15/s, 1e-14/s, 2e-14/s and 2e-13/s and measurement intervals (τ's) of 1, 0.2, 0.1 and 0.01 seconds respectively for a 50 MHz TIC clock. These resolutions can be observed in a plot or histogram of the measured frequency data.

- **Data Averaging**

The DMTDComm program includes provisions for averaging the data as it is captured, either arithmetically (frequency averaging) or decimation (phase averaging). The latter reduces the noise but also changes the statistical properties of the data. Either method reduces the size of the data file.

- **Phase Spillovers**

Phase spillovers in the TIC reading occur at increments of the RF carrier period (e.g., 100 ns for 10 MHz), and can be a problem when there is a significant frequency offset (e.g., a frequency offset of $\Delta f/f = 1x10^{-9}$ at 10 MHz results in a spillover every 100 seconds). The actual span of the TIC is larger by the heterodyne factor, of course (100 ms for a 10 Hz beat frequency). One solution for a stable source is to use a DDS as the RF reference, but a better solution is to replace the time interval counter with a time tagger and obtain the time interval as the difference between the measurement and reference channel time tags. The DMTDComm program is able to remove a reasonable number of phase spillovers from the data stream, resulting in a continuous phase record having a gap at each spillover. This "sawtooth correction" detects a phase change greater than half of full scale and adds or subtracts the known full scale amount from all subsequent readings. Because the exact spillover time is not known, a gap (zero value) is inserted in place of the reading at that point.

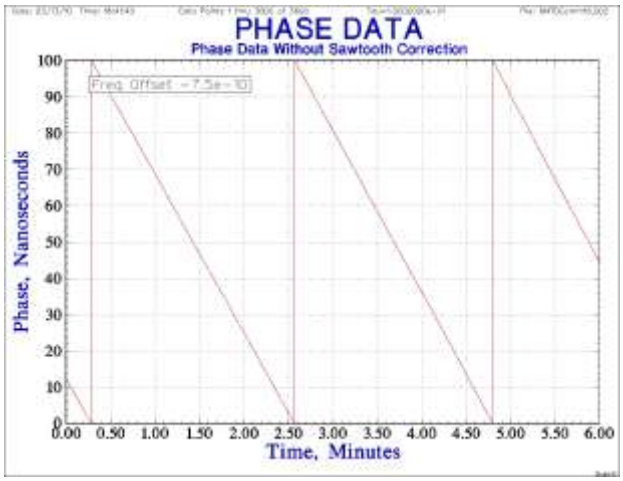


Figure 35. Phase Data w/o Sawtooth Correction

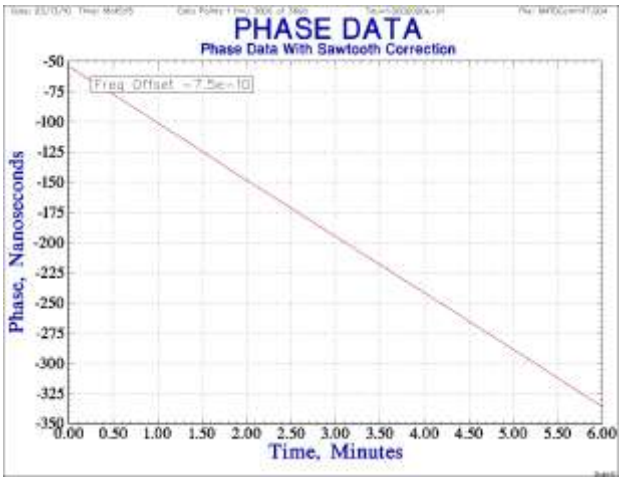


Figure 36. Phase Data with Sawtooth Correction

Figure 35. shows the uncorrected phase record for a small OCVCXO having a frequency offset of ≈ -7.5×10^{-10}. Phase spillovers occur with a period of about 100 ns/7.5e-10 = 133 s = 2.2 min. Figure 36 shows a later portion of the same run with the sawtooth correction activated, which produces a smooth phase record. The corresponding frequency record in Figure 37 shows no effect from the phase spillover.

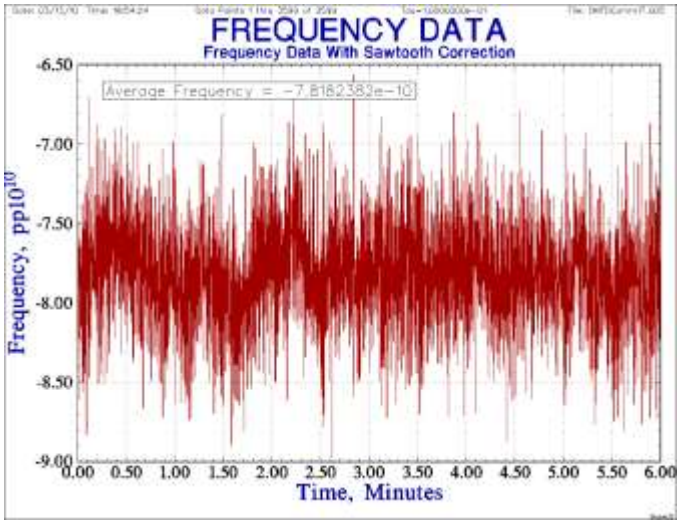


Figure 37. Freq Data with Sawtooth Correction

- **Crosstalk Effects**

The most problematic crosstalk observed was between 10 MHz RF inputs and the 50 MHz PICTIC clock. That coupling can cause an aliased low frequency beat in the measured phase difference that depends on the exact TIC clock rate. A system with higher resolution would require better modular packaging, better shielding and perhaps optical isolation of the TIC start and stop signals.

- **Outliers**

The Small DMTD data are reasonably outlier-free even at high data rates and over long observation times. Outliers that have values near the midpoint of the time interval counter do occur occasionally in the B section, and their cause is still under investigation.

- **Sense and Accuracy**

The sense and accuracy of the Small DMTD system was confirmed by applying a coherent input signal from a 48-bit DDS having a nominal $+1 \times 10^{-11}$ frequency offset from 10 MHz. The #1 and #3 inputs correspond to the measurement channels of the A and B sections, producing positive-going phase ramps. The measured average frequency offsets agreed closely with the expected value.

RF Drive Level Sensitivity

As expected, a lower RF drive level degrades the coherent noise floor, as shown in Figure 38. These evaluations were done with the right (A) section internal RF gain adjustment set with a nominal +7 dBm input for the largest (≈ 6.8 V p-p) undistorted sine wave IF signal after the first amplifier stage, giving a 0.25 V/ms slew rate at its zero crossings. The left (B) section gain set to maximum which produces a distorted ≈ 8.3 V p-p IF signal having a higher 0.40 V/ms slew rate. The distortion is produced in the mixer; the amplifier is not saturated. The corresponding slew rates of the trapezoidal second stage output at the comparator inputs are 2.0 and 4.0 V/ms. Clearly, the B section (red curve) is better as the RF drive level is reduced from its +7 dBm nominal.

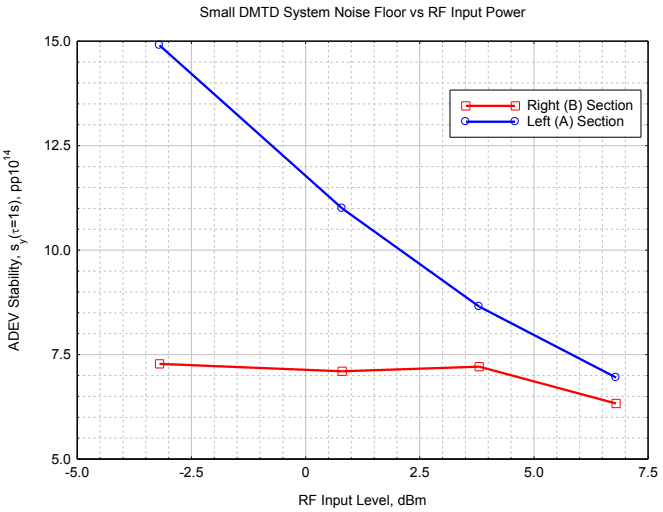


Figure 38. Noise Floor vs. RF Input Power

Time Tagging

Time tagging would be better than time interval counting as the means for measuring the phase difference between the measurement and reference clocks, and is under consideration as an alternative to the PIC TIC in this design. The major advantages would be elimination of sawtooth phase spillovers and TIC the dead zone, and the ability to easily measure any channel against any other channel.

Thermal Considerations

Small, slow phase changes do not appreciably affect frequency stability results, so, if that is the measurement objective rather than phase per se, then normal laboratory temperature changes are not a serious problem. A major source of temperature sensitivity, phase offset in the mixer diodes, has been eliminated by AC coupling in the IF amplifier before the zero-crossing detector. No definitive phase versus temperature measurements have been made.

Mechanical Considerations

One picosecond corresponds to a distance of 0.3 mm in air, so a phase difference of 1e-13 second requires only 0.03 mm of mechanical displacement. This obviously means that all RF connections must be very rigid. No RF connectors are used inside the Small DMTD unit, but the external BNC connectors are subject to mechanical disturbance and must not be allowed to move during a measurement.

Measurement Example

As an example of an actual measurement with the Small DMTD system, consider the comparison between two Datum LPRO commercial rubidium oscillators [26] for which $\tau = 0.1$ second data were collected for one day, as shown in Figures 39-42..

Figure 39. Phase Record

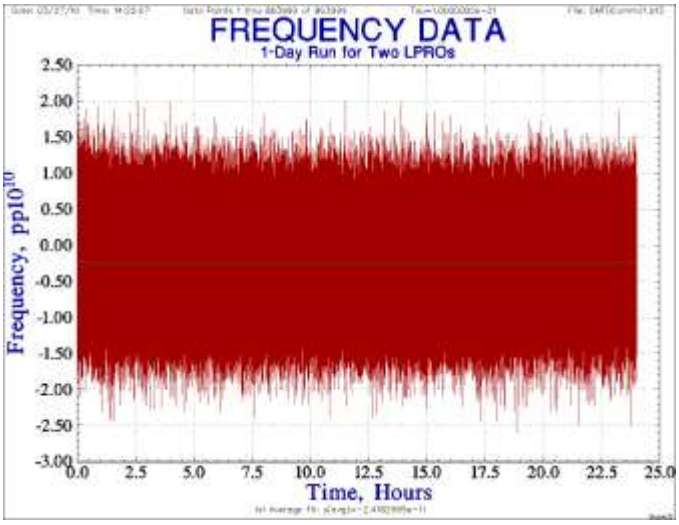
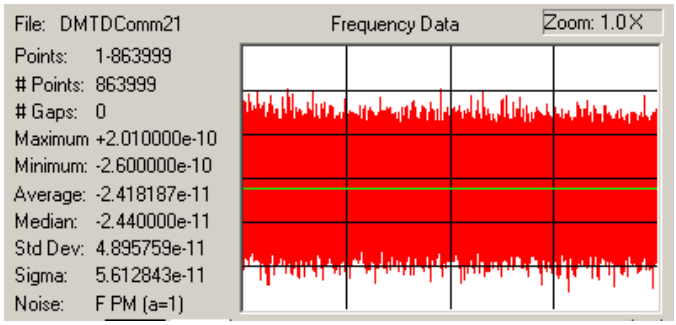


Figure 40. Frequency Record



Linear Frequency Drift = -4.10×10^{-12}/day

Figure 41. Statistics

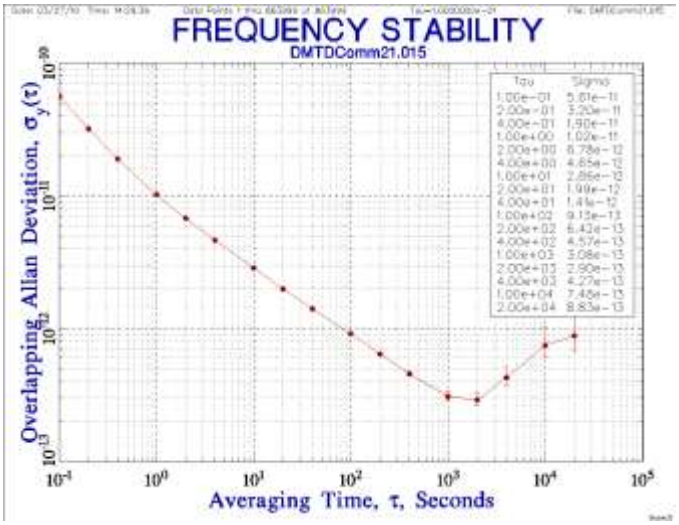


Figure 42. Frequency Stability

The measured short-term stability of these two rubidium oscillators, 1.0×10^{-11} at 1-second, is excellent, x2.5 better than their specification even without correction for two units. Also noteworthy is how close they are in average frequency, about 2.5×10^{-11}, without recalibration after their purchase on the surplus market. Their mutual frequency drift, although quite negligible for this short run, isn't particularly meaningful because one of the units was turned on a few hours before the run began.

A longer 30-day run was then conducted to better establish their "flicker floor" at the averaging time where the stability reaches its best value. The frequency of one of the units was adjusted close to zero-beat with respect to the other at the start of the run. The raw phase record, outlier-removed frequency record and drift-removed ThêoH stability plot for the run are shown in Figures 43-45. The phase record had one gross discontinuity caused by a power line transient during a thunderstorm. The relative frequency drift between these two mature rubidium oscillators was 2.5×10^{-13}/day. Their combined short-term white FM noise is an excellent $\sigma_y(\tau)=8.6 \times 10^{-12}$, their medium-term instability peaks in the 1000 second region, presumably due to temperature sensitivity and air conditioner cycling, and their long-term flicker FM noise floor is about 2×10^{-13}, a typical value for these devices.

Figure 43. Raw Phase Record

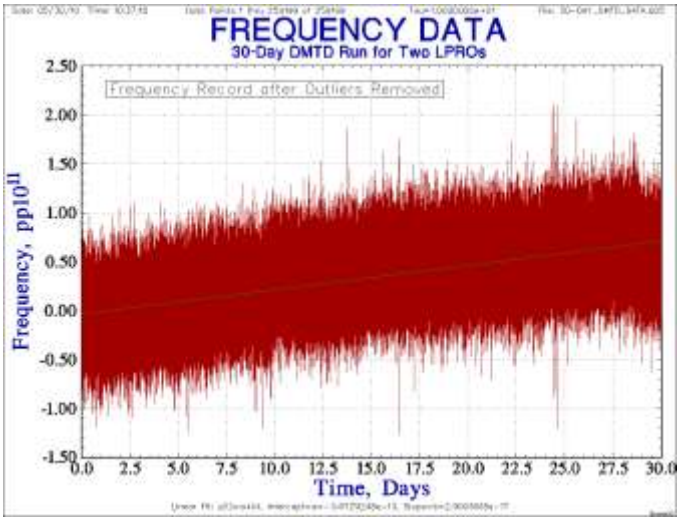


Figure 42. Outlier-Removed Frequency Record

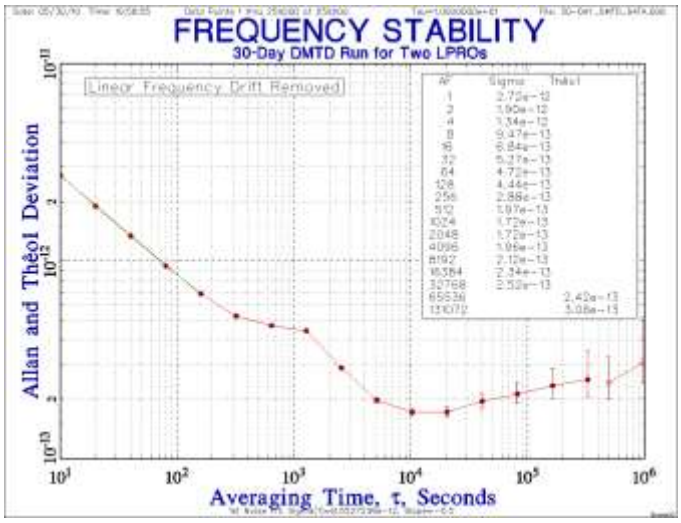


Figure 42. Drift-Removed Frequency Stability

Conclusion

The Small DMTD system has satisfied its objective as a simple, high-resolution clock measuring instrument.

Acknowledgement

I wish to acknowledge the interest and kind assistance of Richard McCorkle with the PICTIC time interval counter used in this project.

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Appendix I

Preliminary Specifications for Small DMTD Clock Measuring System		
Parameter	**Specification**	**Remarks**
RF Frequency Range	1-20 MHz	Can be extended in either direction
RF Input Level	0 to +7 dBm	Uncritical
RF Input Impedance	50 Ω nominal	Internally isolated
Standard RF Frequencies	5, 10, 10.23 and 13.40134393 MHz	Can be changed via optional DDS Module user interface
Standard Beat Frequencies	1, 5, 10 and 100 Hz	
Measurement Tau	1, 0.2, 0.1 and 0.01 second	Determined by beat frequency
# RF Channels	2 pairs	2 independent DMTD sections
# Time Interval Counters	2	Expandable to 3
# RF Power Splitters	2	2-way
DDS and TIC Reference	10 MHz	Sets beat frequency and scale factor
Resolution	20 femtoseconds	At 10 MHz with 10 Hz offset
Noise Floor	ADEV < $1x10^{-13}$ at 1-second	W/O averaging or cross-correlation
Measurement options	Phase decimation and averaging	Using DMTDComm
	Cross-correlation	Using Stable32
RF Connectors	BNC	4 RF, 6 splitter, 1 reference
Controls	Run/Start clock toggle switch	To start and stop all measurements
	Frequency select switch	Internal 4-bit DIP switch
Data Interface	USB 2.0 Virtual COM Port	Stable32 compatible format
Data Rate	57600 Baud	2 or 3 channels
Data Connector	USB Type B	Internal USB hub
Software	DMTDComm	Included (control and data capture)
	Stable32	Recommended (analysis)
PC Compatibility	Microsoft Windows®	Any 32-bit version
Size (L x W x H)	8” x 12” x 4”	Excluding 4.5” x 3.0” x 2.5”, 2.6 lb external power supply
Weight	4.6 lbs	
Power	120 VAC, 60 Hz, TBD W	+5 VDC and ±12 VDC internal from external T512100/37 power supply with 5-pin DIN connector
Availability	Not for sale	Contact Hamilton Technical Services

Appendix II

The Influence of Offset LO Noise and Nominal Phase Difference on the Small DMTD Noise Floor

- **Introduction**

The noise floor of a DMTD clock measuring system depends on the noise of its offset local oscillator and the degree which that noise is cancelled [7, 8]. The former depends on the quality of the LO source while the latter is improved by minimizing the nominal phase difference between the start and stop signals from the two mixer channels. This appendix shows the dependence of the Small DMTD system noise floor on nominal phase difference for a DDS offset LO and an alternative offset crystal oscillator LO.

- **Effect of Nominal Phase Difference**

The noise floor of the original Small DMTD system with its DDS offset LO is very sensitive to the phase difference between its two channels. Like many cancellation or nulling processes, the minimum noise occurs at a particular condition and degrades rapidly away from it. This is shown in Figure 1, where the nominal phase difference must be below about 1 ns to achieve a noise floor under $1x10^{-13}$ at 1 second, while, at the other extreme of large phase differences, the noise is more than an order-of-magnitude larger but less sensitive to the phase difference.

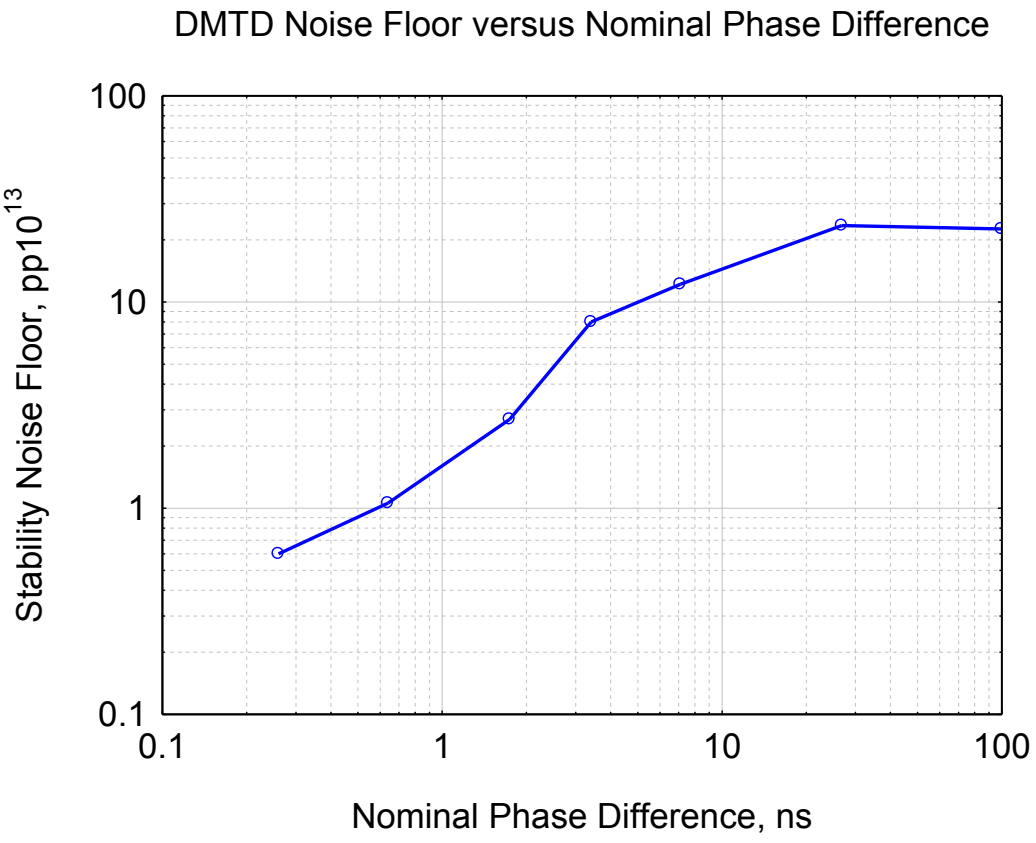

Figure 1. Small DMTD Noise Floor versus Nominal Phase Difference for DDS LO

- **Effect of LO Stability**

The DMTD noise floor scales with the LO stability at the sampling time of the measuring system. This LO noise, typically white PM noise for a DDS offset LO synthesizer or flicker FM noise from an offset crystal oscillator, is reduced by the cancellation that occurs at small phase differences. Thus a lower noise LO source is particularly advantageous when a small phase difference cannot be maintained during the measurement.

Low noise ovenized crystal oscillators can provide stabilities between a few $pp10^{12}$ and $1pp10^{13}$ at the sampling times between 0.1 and 1 second used in a typical DMTD system. In contrast, a DDS synthesizer has somewhat poorer short term stability, but it offers coherency with an external reference. The autocorrelation function of the white FM VCXO noise extends to longer lags than does the white PM DDS noise.

- **DDS Noise**

The measured noise of a DDS synthesizer similar to that used in the Small DMTD system is shown in Figure 2. These data were taken using the Small DMTD system with an HP 10811 OCVCXO as the common reference source which has a measured 1-second stability of about $2x10^{-12}$. The nominal phase difference was kept under 1 ns to minimize the system noise. The DDS synthesizer noise is about $2x10^{-11}$ at 0.1 second and $6x10^{-12}$ at 1 second.

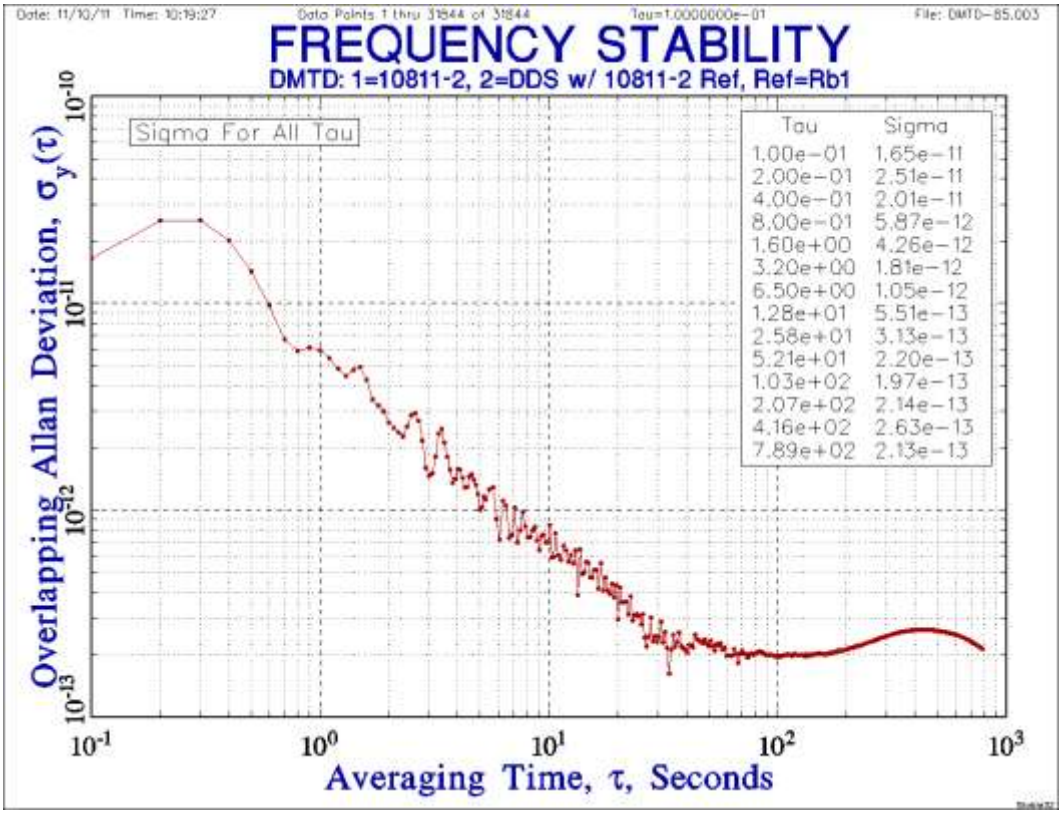

Figure 2. Stability Plot for DDS Synthesizer

Small DMTD System Input 1 = HP 10811 OCVCXO #2, DMTD Input 2 = DDS Synthesizer with HP 10811 #2 Reference, DMTD Reference Input = LPRO Rb #1, all at nominal 10 MHz. DDS Hex Word = 155555555555 with 120 MHz clock. Nominal phase Difference = 0.3 ns.

Another measurement was made using the same setup but with a fairly slow (0.2 second time constant) HP 10811 OCVCXO PLL cleanup loop after the DDS [9]. Those results, shown in Figure 3, show the improvement possible with that arrangement. The DDS synthesizer noise is about $1x10^{-11}$ at 0.1 second and $4x10^{-12}$ at 1 second. A slower PLL should be even better.

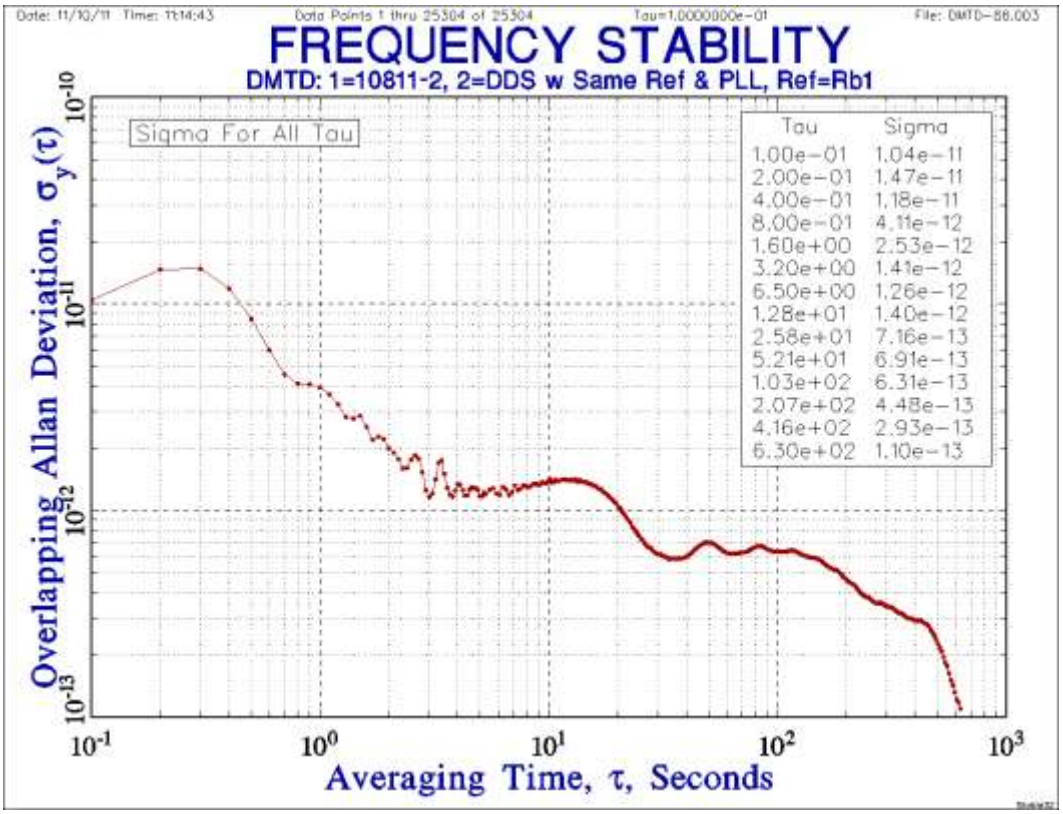

Figure 3. Stability Plot for DDS Synthesizer with OCVCXO PLL Cleanup Loop

Small DMTD System Input 1 = HP 10811 OCVCXO #2, DMTD Input 2 = DDS Synthesizer with HP 10811 #2 Reference followed by HP 10811 OCVCXO #1 PLL with 0.2 second time constant, DMTD Reference Input = LPRO Rb #1, all at nominal 10 MHz. DDS Hex Word = 155555555555 with 120 MHz clock. Nominal phase Difference = 0.5 ns.

Excluding its clock, the noise and spurious components of a DDS synthesizer can be attributed to three causes: (a) phase truncation, (b) quantization noise and (c) DAC non-linearity. Item (a) arises because the phase accumulator bits are truncated before accessing the sine lookup table, item (b) arises because of the finite bit size of the DAC, and item (c) is due to "glitches" and other analog defects. In general, all of these noise sources are correlated (i.e., coherent with the clock) and therefore not reducible by cross-correlation. In particular, the phase truncation spurs and quantization noise are highly deterministic and perfectly correlated. Additive thermal white and electronic flicker noise is normally much lower.

- **Cross-Correlation**

A dual channel DMTD system using cross-correlation can lower the measuring system noise floor by cancelling the uncorrelated noise between the two channels. But this does not reduce the offset LO noise because it is common to the two channels. Nor would using two identical DDS synthesizers help because their noise would still be mostly coherent.

Using two DDS synthesizers with different clock multiplier factors and tuning words to produce (almost) the same offset frequency would seem likely to de-correlate their noise, and if their frequency difference is very small it would probably not be a problem. A pair of high-resolution 48-bit DDS would be needed. For example, for a +10 Hz offset at 10 MHz, 48-bit DDSs clocked at 10 MHz using clock multipliers of x11 and x12 would use hex tuning words of 1745D2FAD0B2 and 155556BB3F4D and have a fractional frequency difference with respect to 10 MHz of about 3.553×10^{-14}, about 3.07 ns per day.

But of those approaches require both more complicated hardware and processing and their effectiveness is uncertain.

Several authors have proposed and investigated schemes for reducing DDS noise by using an array of those devices in which their correlated carrier powers add while their uncorrelated noise and spurs do not and are therefore suppressed [1-6]. It is unclear, however, exactly why and to what degree the noise of two DDS synthesizers is uncorrelated. One such scheme applies different pseudo-random phase modulation signals to each DDS to insure noise de-correlation but this requires many elements to make an improvement.

Introducing a constant phase shift between two DDS synthesizers does tend to decorrelate their noise, and the sampling noise becoming uncorrelated when the phase difference is an odd multiple of 90° [4]. This carrier phase shift is not acceptable in an ordinary DMTD configuration unless it is removed afterwards, or by a quadrature I-Q type RF processor.

- **PLL OCVCXO Cleanup Loop**

It is possible to use a low-noise OCVCXO in a slow PLL to clean up the short-term stability of a DDS (albeit at a single nominal frequency). The OCVCXO must have good stability (e.g., a few $pp10^{12}$) at the sampling time of the DMTD system (e.g., 0.1 second), and the PLL loop time constant must be an order-of-magnitude slower than that (e.g., 1 second). It must also have respectable thermal stability over averaging times at least as long as the loop time constant. A 1st-order PLL with minimal DC gain (only enough to produce the required control voltage) is suitable and easy to implement without large component values. Two such offset LO sources could support cross-correlation noise reduction because the noise of the two OCVCXOs would be uncorrelated. A candidate for a 10 MHz + or – 10 Hz offset OCVCXO for that application is the Milliren 250 Series, a 2" x 2" x 1" plug-in device available with an SC-cut crystal and having 2×10^{-12} short-term stability similar to the larger HP 10811. Otherwise, the cleanup PLL circuit would be similar to that of the HP 10811 10 MHz OCVCXO and PLL module used in the testing above.

- **Incoherent Offset OCVCXO**

The offset LO does not necessarily have to be coherently referenced to a frequency standard. A free-running low-noise OCVCXO can be used as the offset source in a multi-channel system where the resulting data for a pair of channels (e.g., UUT and reference) are differenced before analysis thus removing the effect of their common LO. That approach was used in the original Timing Solutions TSC 3020 clock measuring system. The main disadvantage is that at least two sources must be measured. Figure 4 shows the measured noise floor of the Small DMTD system with a free-running Milliren 250 Series OCVCXO offset LO. The noise floor is somewhat higher at small phase differences with the 10 MHz +10 Hz OCVCXO offset LO but is nearly an order-of-magnitude better at intermediate phase difference values and has less dependence of the nominal phase difference, remaining below 1×10^{-12} for all phase differences.

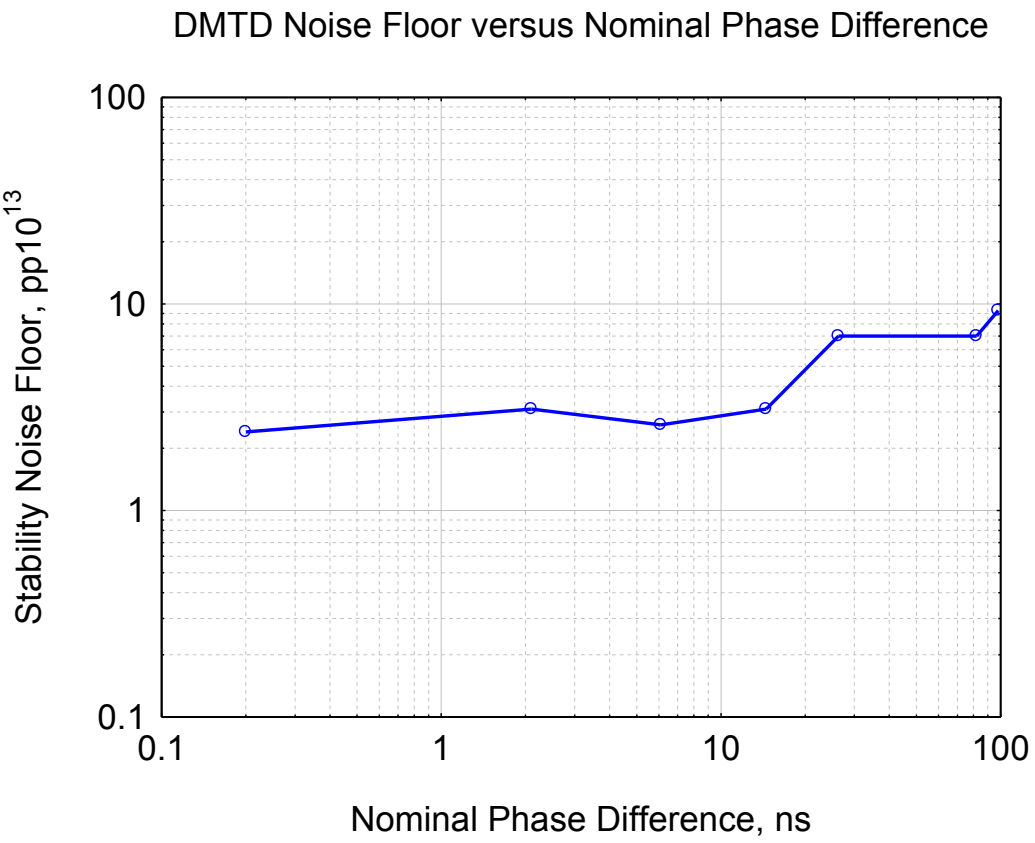

Figure 4. Small DMTD Noise Floor versus Nominal Phase Difference for OCVCXO Offset LO

- **Coherent Offset OCVCXO Pair**

A pair of offset OCVCXOs coherently phase locked in a slow PLL to the same DDS synthesizer would have not only relatively low noise but their noise would be uncorrelated and thus could be significantly reduced by using cross-correlation. That combination is potentially the best offset LO arrangement, especially one that has to work at large phase differences.

- **Conclusion**

The coherent DDS offset LO is best when measuring highly-stable syntonized sources such as atomic frequency standards that can be adjusted for and can maintain a small nominal phase difference, while an incoherent OCVCXO offset LO is recommended for measuring sources that cannot maintain that condition.

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